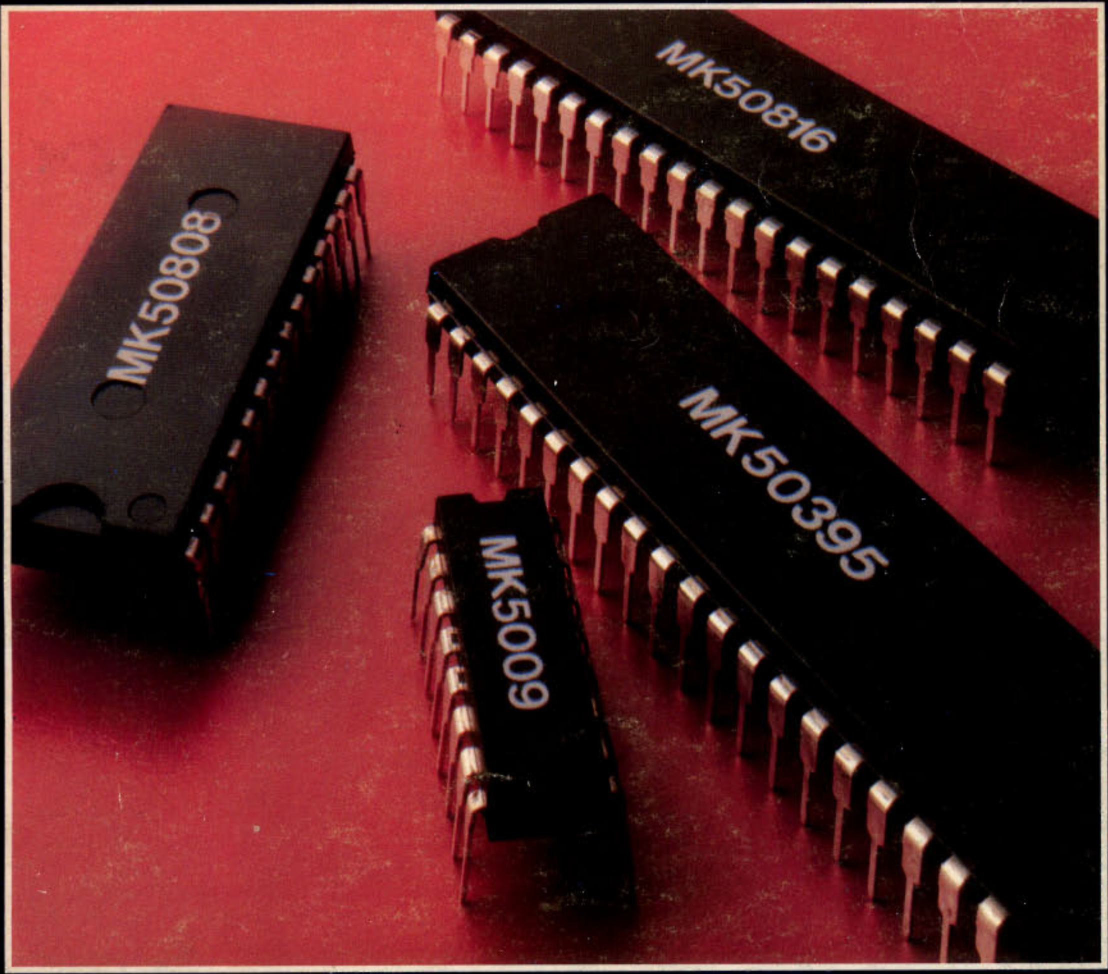
MOSTEK 1980

INDUSTRIAL PRODUCTS DATA BOOK



1980
INDUSTRIAL PRODUCTS
DATA BOOK

Ex-Libris
Arthur Missira
MCMXCVII

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STD No. 20003

1980 INDUSTRIAL PRODUCTS DATA BOOK

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***Not Recommended for New Design**

NUMERICAL INDEX

*Not Recommended For New Design

1980 INDUSTRIAL PRODUCTS DATA BOOK

ORDERING INFORMATION

Factory orders for parts described in this book should include a four-part number as explained below:

Example: MK 5009 P - 3

1. Dash Number
2. Package
3. Device Number
4. Mostek Prefix

1. Dash Number

   One or two numerical characters defining specific device performance characteristic.

2. Package

   P - Gold side-brazed ceramic DIP
   J - CER-DIP
   N - Epoxy DIP (Plastic)
   K - Tin side-brazed ceramic DIP
   T - Ceramic DIP with transparent lid
   E - Ceramic leadless chip carrier

3. Device Number

   1XXX or 1XXXX - Shift Register, ROM
   2XXX or 2XXXX - ROM, EPROM
   3XXX or 3XXXX - ROM, EPROM
   38XX - Microcomputer Components
   4XXX or 4XXXX - RAM
   5XXX or 5XXXX - Counters, Telecommunication and Industrial
   7XXX or 7XXXX - Microcomputer Systems

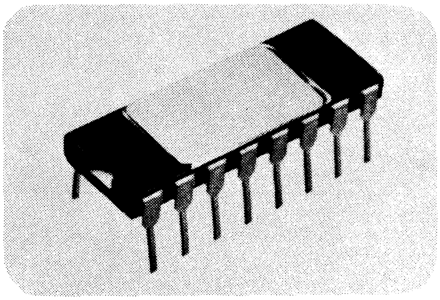
4. Mostek Prefix

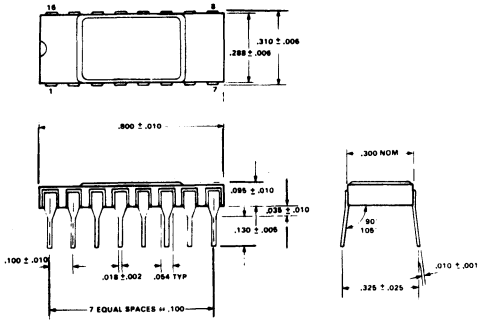
   MK-Standard Prefix

   MKB-100% 883B screening, with final electrical test at low, room and high-rated temperatures.

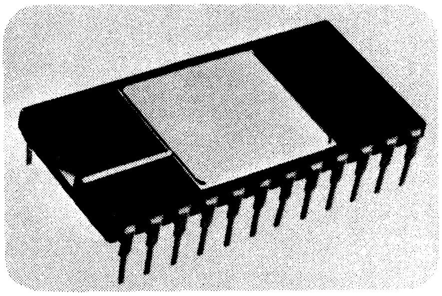
Package Descriptions

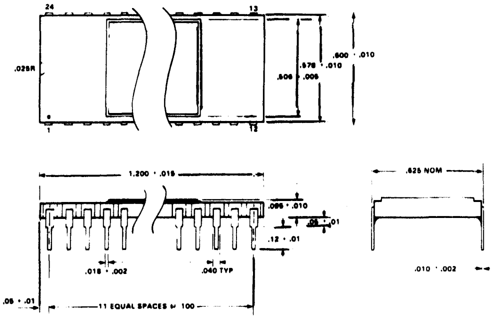
Ceramic Dual-In-Line Package (P)
16 Pin





Ceramic Dual-In-Line Package (P)
24 Pin





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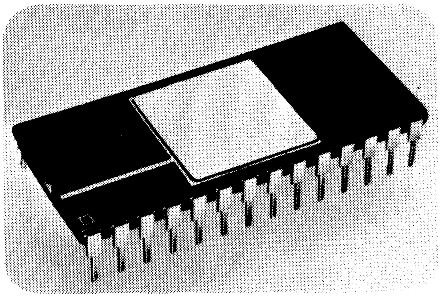
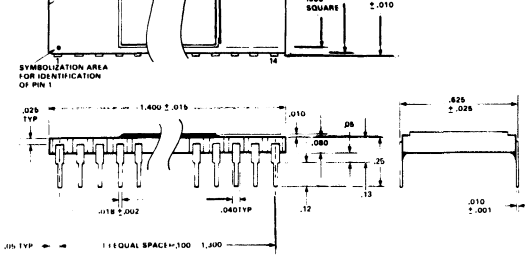
28 Pin





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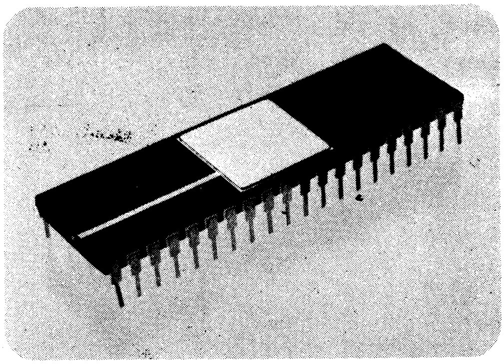
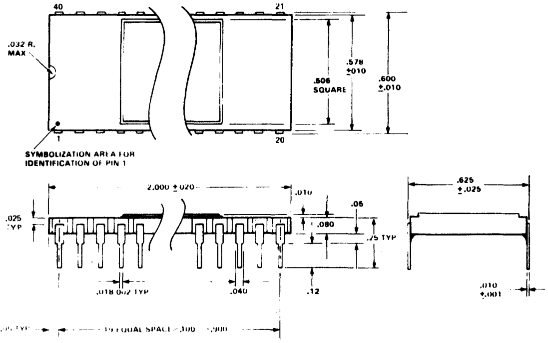
40 Pin





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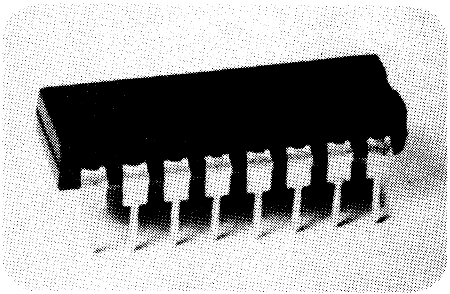
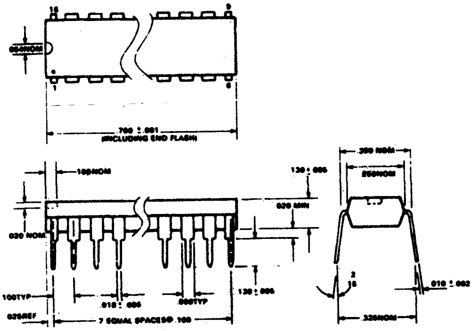
16 Pin





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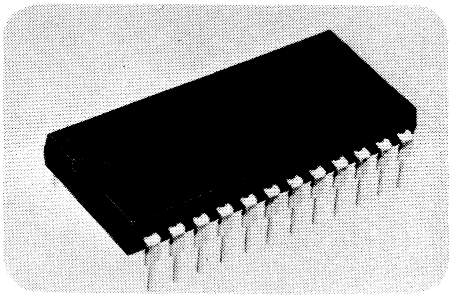

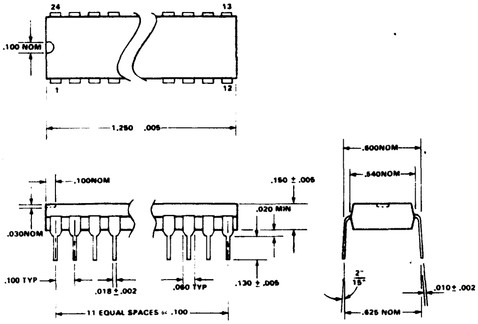

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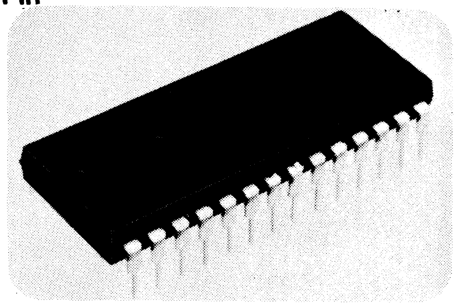

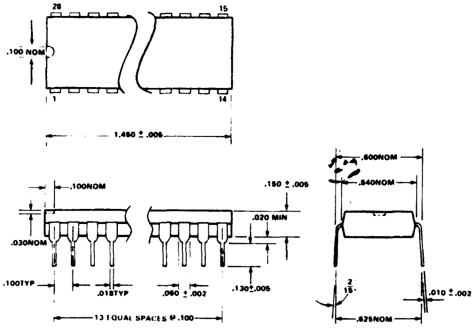

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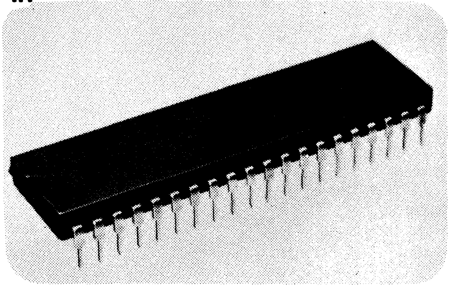
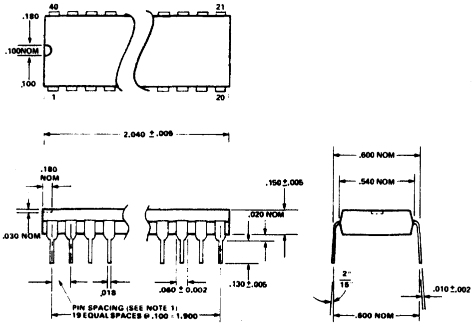
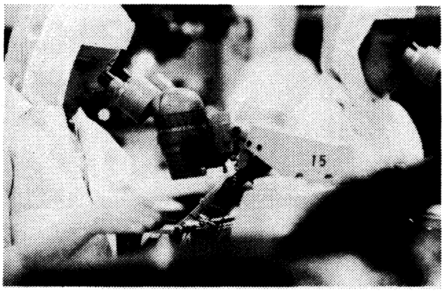
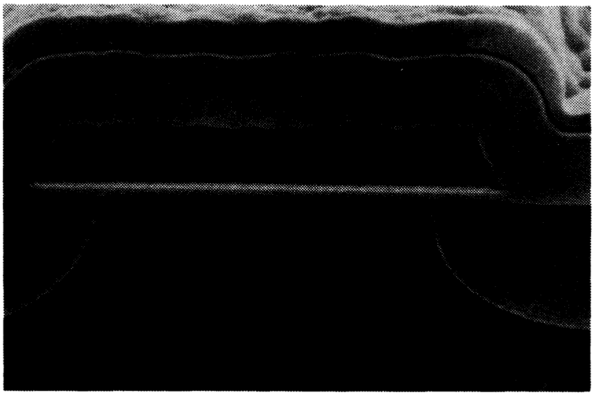
40 Pin

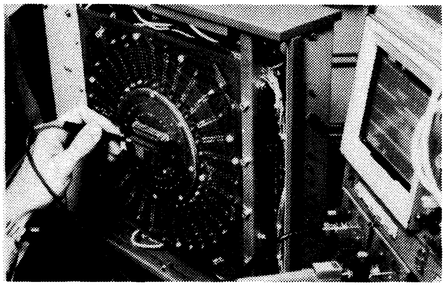




Mostek - Technology For Today And Tomorrow







TECHNOLOGY

From the beginning, Mostek has been recognized as an innovator. In 1970, Mostek developed the MK4006 1K dynamic RAM and the world's first single-chip calculator circuit, the MK6010. These technical breakthroughs proved the benefits of ion-implantation and cost-effectiveness of MOS. Now, Mostek represents one of the industry's most productive bases of MOS/LSI technology. Each innovation - in memories, microcomputers and telecommunications - adds to that technological capability.

QUALITY

The worth of a Mostek product is measured by its quality. How well it's designed, manufactured and tested. How well it works in your system.

In design, production and testing, our goal is meeting the spec every time. This goal requires a strict discipline, both from the company and from the individual. This discipline, coupled with a very personal pride, has driven Mostek to build in quality at every level, until every product we take to the market is as well-engineered as can be found in the industry.

PRODUCTION CAPABILITY

Mostek's commitment to increasing production capability has made us the world's largest manufacturer of dynamic RAMs. In 1979 we shipped 25 million 4K and 16K dynamic RAMs. We built our first telecommunication tone dialer in 1974; since then, we've shipped over 5 million telecom circuits. The MK3870 single-chip microprocessor is also a large volume product with over two million in application around the world. To meet the demand for our products, production capability must be constantly increased. To accomplish this, Mostek has been in a constant process of expanding and refining our production capabilities.

THE PRODUCTS

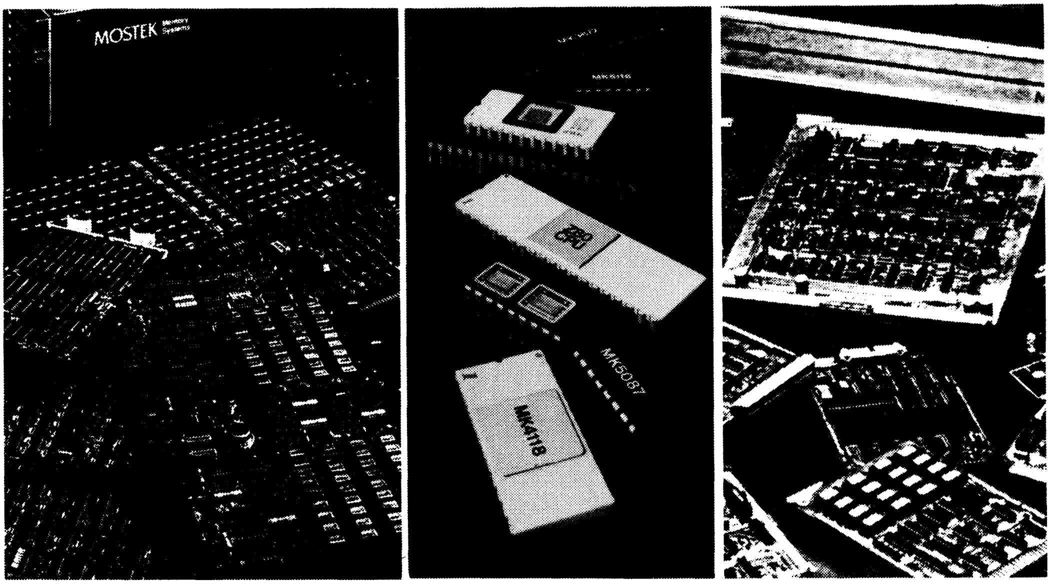
Telecommunications and Industrial Products

Mostek has made a solid commitment to telecommunications with a new generation of products, such as Integrated Pulse Dialers, Tone Dialers, CODECs, monolithic filters, tone receivers, A/D converters and counter time-base circuits.

Since 1974 over five million telecom circuits have been shipped, making Mostek the leading supplier of tone/pulse dialers and CODECs.

Memory Products

Through innovations in both circuit



design, wafer processing and production, Mostek has become the industry's leading supplier of memory products.

An example of Mostek leadership is our new BYTEWYDE™ family of static RAMs, ROMs, and EPROMs. All provide high performance, N words x 8-bit organization and common pin configurations to allow easy system upgrades in density and performance. Another important product area is fast static RAMs. With major advances in technology, Mostek static RAMs now feature access times as low as 55 nanoseconds. With high density ROMs and PROMs, static RAMs, dynamic RAMs and pseudostatic RAMs, Mostek now offers one of industry's broadest and most versatile memory families.

Microcomputer Components

Mostek's microcomputer components are designed for a wide range of applications.

Our Z80 family is the highest performance 8-bit microcomputer available today. The MK3870 family is one of the industry's most popular 8-bit single-chip microcomputers, offering upgrade options in ROM, RAM, and I/O, all in the same socket. The MK3874 EPROM version supports and prototypes the entire family.

Microcomputer Systems

Supporting the entire component product line is the powerful MATRIX™ microcomputer development system, a Z80-based, dual floppy-disk system that is used to develop and debug software and hardware for all Mostek microcomputers.

A software operating system, FLP-80DOS, speeds and eases the design cycle with powerful commands. BASIC, FORTRAN, and PASCAL are also available for use on the MATRIX.

Mostek's MD Series™ features both standalone microcomputer boards and expandable microcomputer boards. The expandable boards are modularized by function, reducing system cost because the designer buys only the specific functional modules his system requires. All MDX boards are STD-Z80 BUS compatible.

The STD-Z80 BUS is a multi-sourced motherboard interconnect system designed to handle any MDX card in any card slot.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC and Data General minicomputers.

Mostek also offers special purpose and custom memory boards for special applications.

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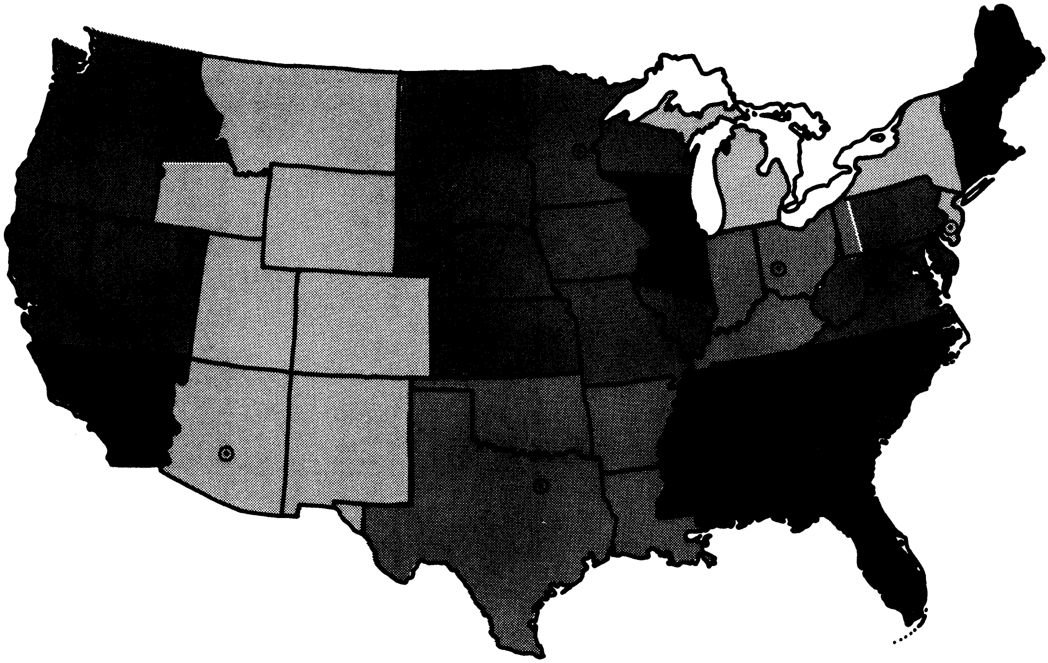

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1980 INDUSTRIAL PRODUCTS DATA BOOK

MOSTEK®

TOP OCTAVE FREQUENCY GENERATOR

MK50240/1/2

FEATURES

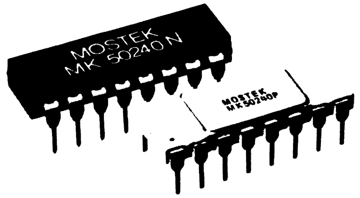
☐ Single Power Supply

☐ Broad Supply-Voltage Operating Range

☐ Low Power Dissipation

☐ High Output-Drive Capability

☐ MK 50240 — 50% Output Duty Cycle
MK 50241 — 30% Output Duty Cycle
MK 50242 — 50% Output Duty Cycle



DESCRIPTION

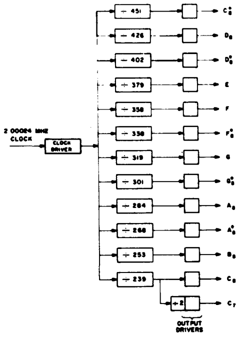
The MK 50240 is one of a family of ion-implanted, P-channel MOS synchronous frequency dividers.

Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal-tempered scale.

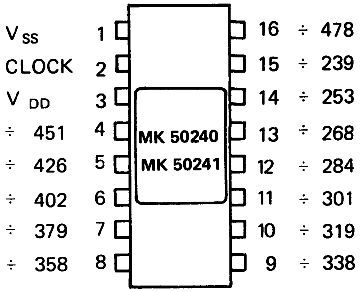
Low threshold-voltage enhancement-mode, as well as depletion-mode devices, are fabricated on the same chip allowing the MK 50240 family to operate from a single, wide-tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 600mW of power. The circuits are packaged in 16-pin dual-in-line packages.

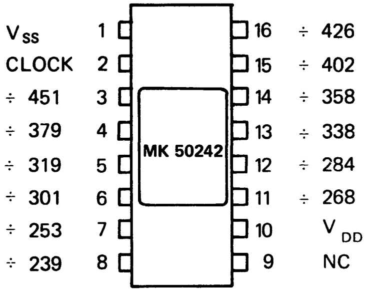
RFI emanation and feed-through is minimized by placing the input clock between the VDD and VSS pins. Internally, the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise-time under no load conditions to reduce the RF harmonic content of each output signal.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS





ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . +0.3V to –20V

Operating Temperature (Ambient) . . . . .0°C to 50°C

Storage Temperature (Ambient) . . . . –40°C to 100°C

RECOMMENDED OPERATING CONDITIONS

($0℃ \leqslant T_A \leqslant 50℃$)

PARAMETER		MIN	TYP	MAX	UNITS	FIGURE
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	–11.0	–15.0	–16.0		

ELECTRICAL CHARACTERISTICS

($0°C \leqslant T_A \leqslant 50°C$; $V_{SS} = 0$, $V_{DD} = -11$ to $-16V$ unless otherwise specified)

PARAMETER		MIN	TYP	MAX	UNITS	FIGURE
V_{IL}	Input Clock, Low	0		–1.0	V	FIG. 1
V_{IH}	Input Clock, High	$V_{DD} + 1.0$		V_{DD}	V	
f_I	Input Clock Frequency	100	2000.240	2500	kHz	
t_r , t_f	Input Clock Rise & Fall Times 10% to 90% @ 2.5 MHz			30	nsec	FIG. 1
t_{on} , t_{off}	Input Clock On and Off Times @ 2.5 MHz		200		nsec	FIG. 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ 0.70 mA	$V_{DD} + 1.5$		V_{DD}	V	FIG. 2
V_{OL}	Output, Low @ 0.75 mA	$V_{SS} - 1.0$		V_{SS}	V	FIG. 2
t_{ro}, t_{fo}	Output Rise & Fall Times, 500 pF Load	250		2500	nsec	FIG. 3
t_{on}, t_{off}	Output Duty Cycle MK 50240P & MK 50242P MK 50241P (Pin 16 50%)		50 30		% %	
I_{DD}	Supply Current		24	37	mA	outputs unloaded

INPUT CLOCK WAVEFORM

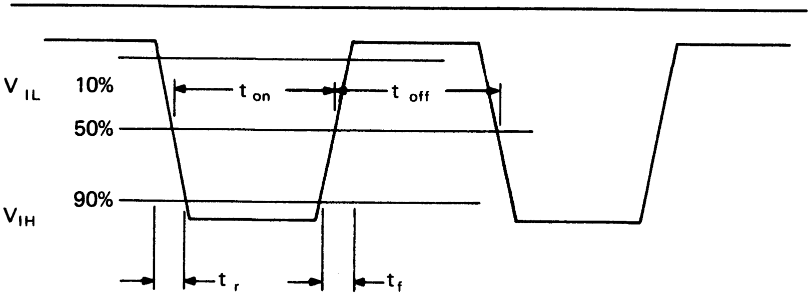


Figure 1

OUTPUT SIGNAL D. C. LOADING

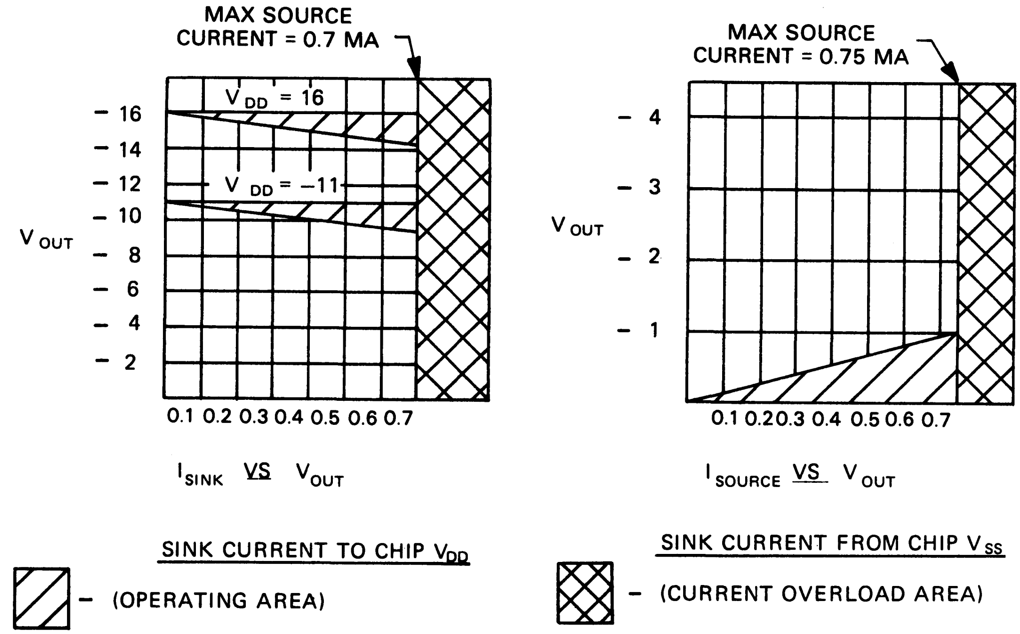
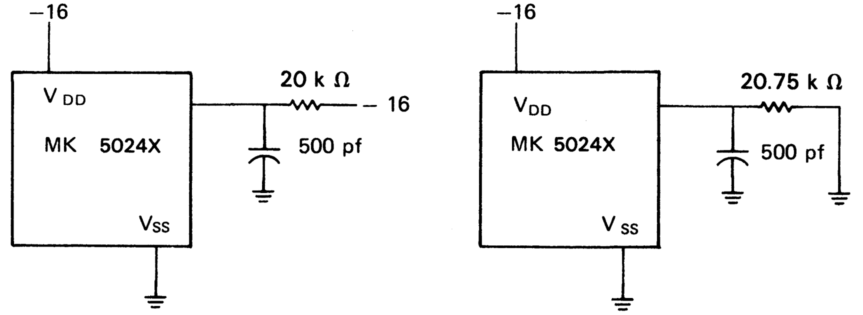


Figure 2

OUTPUT LOADING



t_{fo} Test

t_{ro} Test

Figure 3

1980 INDUSTRIAL PRODUCTS DATA BOOK

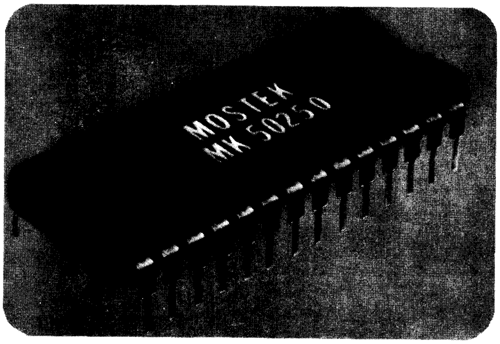
MOSTEK®

MOS DIGITAL ALARM CLOCK

MK50250 Series

FEATURES

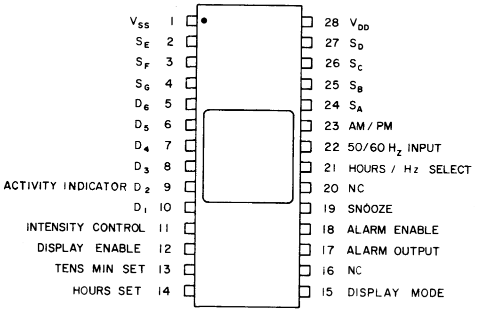
- ☐ Single-Voltage Power Supply
- ☐ Intensity Control
- ☐ Simple Time Setting
- ☐ 4-or 6-Digit Display
- ☐ AM/PM and Activity Indicator
- ☐ Selectable Input Frequency and Output Mode
  - MK 50250 — 12 hr/60Hz or 24 hr/50Hz
  - MK 50253 — 12 hr/50Hz or 24 hr/50Hz
  - MK 50254 — 12 hr/60Hz or 24 hr/60Hz
- ☐ 24 Hr. Alarm
- ☐ Snooze Alarm



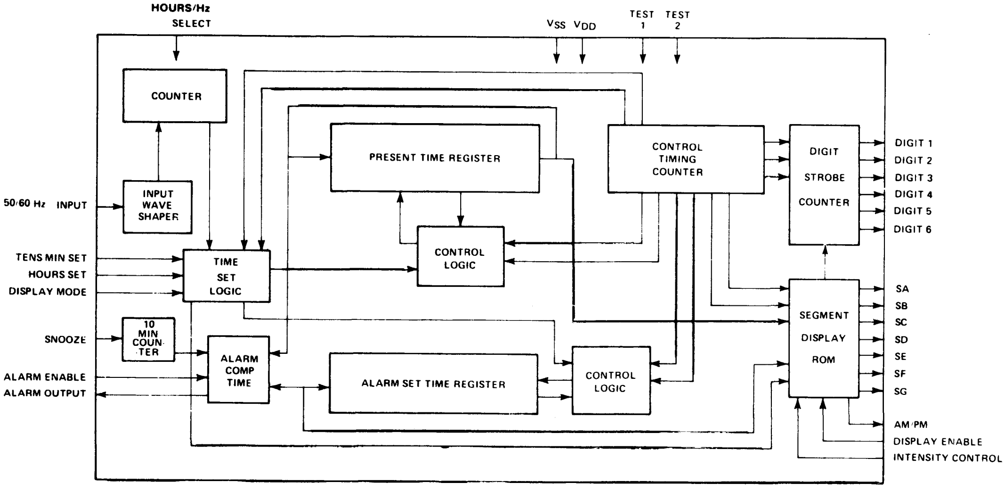
DESCRIPTION

The MK50250 is a versatile MOS/LSI clock circuit manufactured by Mostek using its depletion-mode, ion implantation process and P-channel technology. The circuit can be used to construct a digital alarm clock with the addition of only a simple power supply, display, and standard interfacing components. (See Typical Circuit Configuration). The circuit is compatible with 4- or 6-digit seven-segment multiplexed displays. An AM/PM and circuit activity signal is generated by the chip. The alarm operates in a 24-hour mode, which allows the alarm to be disabled and immediately reenabled to activate 24 hours later. The snooze inhibits an activated alarm for 10 minutes.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



NOT RECOMMENDED FOR NEW DESIGN

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE—AIR TEMPERATURE RANGE

Voltage on any pin relative to V_{SS} .... +0.3 to −18.0V

Output-Voltage Breakdown on any output relative to V_{SS} .... −18.0V @ 10 µA

Operating Free-Air Temperature Range..0°C to 55°C

Storage Temperature Range ....−40°C to + 100°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leqslant T_A \leqslant 55°C$)

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Voltage V_{DD} Relative to V_{SS}	−18.0	−9.0	volts	9
Input Logic Levels				1, 2
"1" Logic Level	$V_{SS}-0.3$	$V_{SS}+0.3$	volts	
"0" Logic Level	−18.0	$V_{DD}+0.5$	volts	

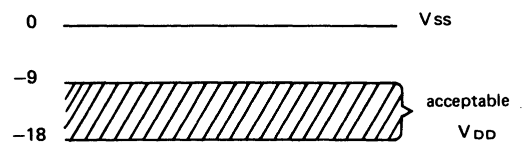
ELECTRICAL CHARACTERISTICS ($9V \leqslant V_{SS} - V_{DD} \leqslant 18V$, $0°C \leqslant T_A \leqslant 55°C$)

PARAMETER	MIN	MAX	UNITS	NOTES
Output Current				
S_A-S_G, D_6-D_1, AM/PM				
"1" Logic Level	0.5		mA	3
"0" Logic Level				4
Alarm Output Current				
"1" Logic Level	0.5		mA	3
"0" Logic Level	−5.0		µA	5
Supply Current, I_{DD}		10	mA	8
Input Current				
Tens Min Set, Hours Set	50	1000	µA	6
Hours/Hz Select	5	100	µA	
Alarm Enable,Snooze	5	100	µA	
50/60 Hz Input, Display Enable	−15	−200	µA	7

Notes:
1. 50/60 Hz Input has 3 volts of hysteresis for noise protection.
2. "Display Mode" and "Intensity" are three-state inputs which will self-seek third state if left open.
3. Output voltage equal to V_{SS}-2.0 volts.
4. Open-drain output.
5. Output voltage equal to V_{DD} +4.0 volts.
6. For power-up clear, capacitance to Vss must not exceed 20pF.
7. Pull-up device provided on 50/60 Hz input.
8. Outputs open.
9. Pins 16 and 20 may be tied to V_{SS} or left floating.

OPERATION

The MK 50250 requires a single power supply with a voltage range from 9V $\leqslant$ $V_{SS} - V_{DD} \leqslant 18$.



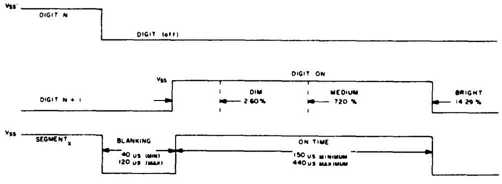
A Three-State Input is one of the features which MOSTEK has employed on the MK 50250 to reduce system expense and simplify operation for the consumer. By switching Display Mode to one of three possible states the mode of operation is as follows:

Display Mode Input	Mode
V_{SS}	Alarm Set
Open	Real Time
V_{DD}	Count Inhibit

When in the Alarm Set mode, the alarm time is displayed and may be altered using the time set procedure (see setting). In the Real Time mode, the real time is displayed and may also be altered using the same procedure. Count inhibit halts the counting of the clock. The display shows the halted time and may be altered by the time set procedure.

The display outputs of the MK 50250 require the use of seven-segment displays which can be multiplexed. The scanning oscillator is completely internal and requires no external components. As can be seen in the timing diagram, each digit is on 14.29% of the time required to scan all 6 possible digits when the intensity mode switch is on bright.

DISPLAY TIMING



NOTES:
1. Display scans digit 1 (unit secs) to digit 6 (tens hr.)
2. Segment polarity is programmable.
3. Blanking the linearly tracks digit on time.

The Intensity Control Input provides the following degrees of display intensity:

Intensity Control Input	Mode	Duty Cycle
V_{SS}	Bright	14.29%
Open	Medium	7.20%
V_{DD}	Dim	2.60%

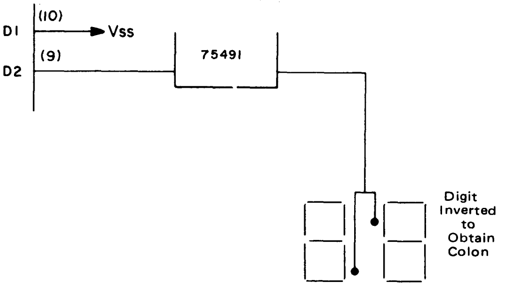
The intensity can be controlled either manually or automatically (see "Automatic Intensity Control" diagram).

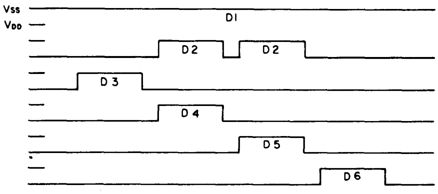
The display can be blanked by connecting the Display Enable input to VDD. Leaving this pin open allows internal pull-up to Vss which enables the display. This feature allows the display to be time shared with other information.

When power is initially applied, both real time and alarm time will be at 12:00:00 midnight in the 12 hr. mode and 00:00:00 in the 24 hr. mode. Time keeping begins when Hrs. Set and Tens Min. set are simultaneously taken to Vss. The units minutes digit can be advanced at a 2 Hz rate by connecting both the Hours Set pin and the Tens Minute Set pin to Vss. This also resets seconds to zero. The Tens Minute digit will advance at a 2 Hz rate when the Tens Minute Set pin is connected to Vss. The hours digit will be advanced by connecting the Hr. Set pin to Vss. The carry from one digit to the next more significant digit does not occur so setting should be performed from the least significant digit to the most significant. Both pins have internal pull-down resistors and can either be left open or tied to VDD when not being used.

The chip can be used with either a 4- or 6-digit display. If digits D1 and D2 are not used to display seconds and tens of seconds, the user is unable to tell if the circuit is active until the minutes digit changes. In order to more quickly determine clock activity, a colon or other indicator can be flashed at a 1 Hz rate by connecting D1 to Vss. D2 can then be used to drive the colon or activity indicator. The D2 output used in this mode occurs during D4 and D5 time so that the decimal point for digits D4 and D5 can be used as a colon.

OPTIONAL ACTIVITY INDICATOR AND TIMING





The AM/PM output operates with an 85% duty cycle at full intensity and conducts to V_{SS} for PM indication.

If a "brown out" occurs, the AM/PM indicator will flash at a 1 Hz rate to signify an incorrect display time. This low power indication continues until proper power is restored and the clock is reset.

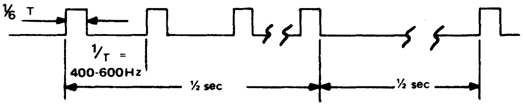
The Hours/Hz Select input is provided with an internal pulldown resistor to VDD. The options available are as follows:

Part	Hours/Hz	Mode
50250	Open or V_{DD}	60Hz - 12 Hrs.
	V_{SS}	50Hz - 24 Hrs.
50253	Open or V_{DD}	50Hz - 12 Hrs.
	V_{SS}	50Hz - 24 Hrs.
50254	Open or V_{DD}	60Hz - 12 Hrs.
	V_{SS}	60Hz - 24 Hrs.

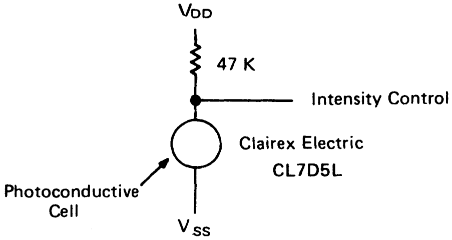
The Alarm Enable pin enables the alarm when connected to Vss. If it is left open, it will disable the alarm due to an internal pull-down resistor to VDD. When alarm occurs it may be disabled and immediately re-enabled and will activate 24 hours later at the alarm time. The output tone will be in the range of 400-600 Hz, and has a 1/6 duty cycle which conducts to Vss 50% of the time at a 1 Hz rate.

The Snooze feature will temporarily turn off an activated alarm signal to allow an additional 10 minutes sleep. Momentarily connecting snooze to Vss will activate the snooze. If left open, an internal pull-down resistor to VDD will maintain the snooze feature inoperative.

ALARM OUTPUT



AUTOMATIC INTENSITY CONTROL



TYPICAL CIRCUIT CONFIGURATION

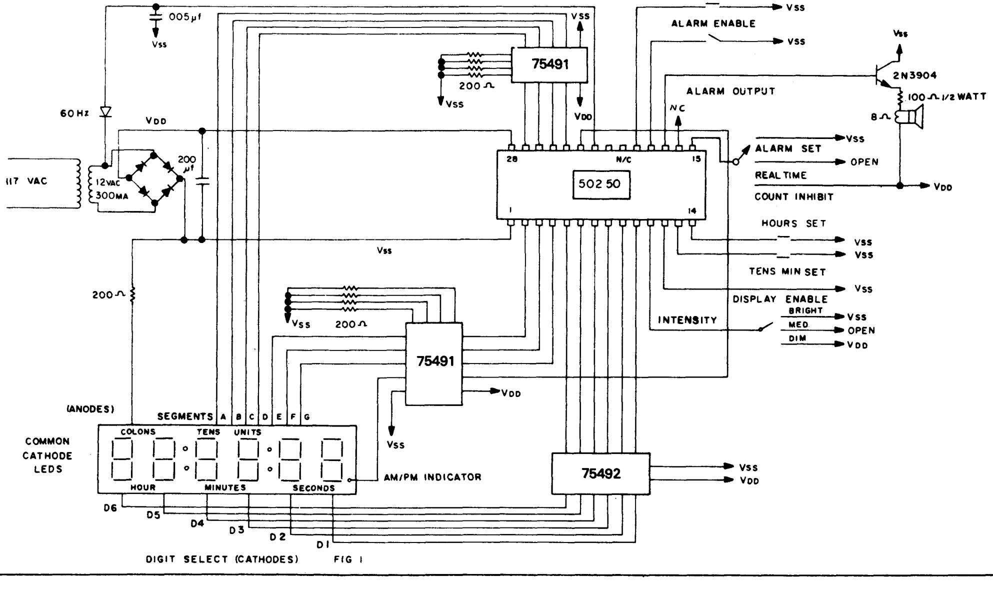


FIG 1

1980 INDUSTRIAL PRODUCTS DATA BOOK

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III Frequency Generator

IV Digital Alarm Clock

V Counter/Display Decoders

VI Counter/Time Base Circuit

VII A/D Converter/Analog Multiplexer

I TABLE OF CONTENTS
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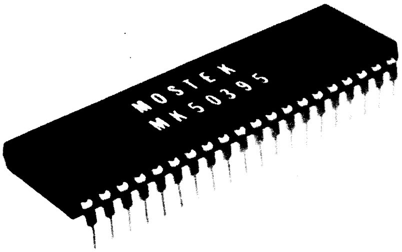
MOSTEK®

SIX DECADE COUNTER / DISPLAY DECODER

MK50395/6/7

FEATURES

- ☐ Single power supply
- ☐ Schmitt Trigger on the count input
- ☐ Six decades of synchronous up/down counting
- ☐ Look-ahead carry or borrow
- ☐ Loadable counter
- ☐ Loadable compare register with comparator output
- ☐ Multiplexed BCD and seven-segment outputs
- ☐ Internal scan oscillator
- ☐ Direct LED segment drive
- ☐ Interfaces directly with CMOS logic
- ☐ Leading zero blanking
- ☐ MK 50396 programmed to count time: 99 hrs. 59 min. 59 sec.
- ☐ MK 50397 programmed to count time: 59 min. 59 sec. 99/100 sec.



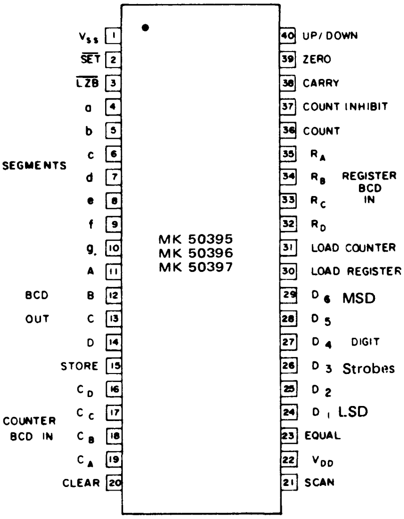
DESCRIPTION

The MK 50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down counter/display driver with compare register and storage latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MK 50396 and MK 50397 operate identically to the MK 50395 except that two digits in each were reprogrammed to provide divide by six circuitry instead of divide by ten. The MK 50396 is well suited for industrial timer applications while the MK 50397 is best suited for stop watch or real-time computer clock applications.

PIN CONNECTIONS FIGURE 1



OPERATIONS:

SIX-DECADE COUNTER, LATCH

The six-decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when the up/down input is high (Vss) and will decrement when the up/down input is low. The up/down input can be changed 0.75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six-digit latch or the scan counter.

As long as the store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when the store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit-by-digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at Vss 2 microseconds prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

INPUTS, OUTPUTS

The seven segment outputs are open drain and capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at Vss. The Carry, Equal, Zero, BCD and digit strobe outputs are push-pull and are on when at Vss. All inputs except Counter BCD, Register BCD, and SCAN inputs are high-impedance CMOS compatible.

Three basic outputs originate from the counter: Zero output, Equal output, and Carry output. Each output goes high on the positive- (Vss) going edge of the count input under the following conditions:

The Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

The Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation, which lasts until the next interdigit blanking period following a negative transition of Load Counter or Load Register.

The Carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999* when counting down and goes low with the negative going edge of the same count input.

A count frequency of 1 MHz can be achieved if the Equal output, Zero output and Carry output are not used. These outputs do not respond at this frequency due to their output delay, as illustrated on the timing diagram, Figure 3.

SIX-DECADE COMPARE REGISTER

The register is loaded identically as described in the load counter paragraph. The register may be loaded independently of the counter. However, the Clear input will not remove the register contents. Contents of the register are not displayed by the BCD or seven-segment outputs.

BCD & SEVEN-SEGMENT OUTPUTS

BCD or seven-segment outputs are available. Digit strobes are decoded internally by a divide-by-six Johnson counter. This counter scans from MSD to LSD. By bringing the SET input low, this counter will be forced to the MSD decade count. During this time, the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when SET is low. Applying Vss to SET allows normal scan to resume. Digit 6 output is active (Vss) until the next scan clock pulse brings up the digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking affects only the segment outputs. This option is disabled by bringing the LZB input high. Typically, the interdigit blanking time is 5 to 25 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore, the BCD output data is valid when the positive transition of a digit output occurs.

SCAN OSCILLATOR

The MK 50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between Vss or VDD and the scan input. The wave form present on the scan oscillator input is triangular in the self-oscillate mode.

An external oscillator may also be used to drive the scan input.

In the internal drive mode, the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self-oscillate blanking time (5 → 25 μsec). Display brightness can be controlled by the duty cycle of the external scan oscillator.

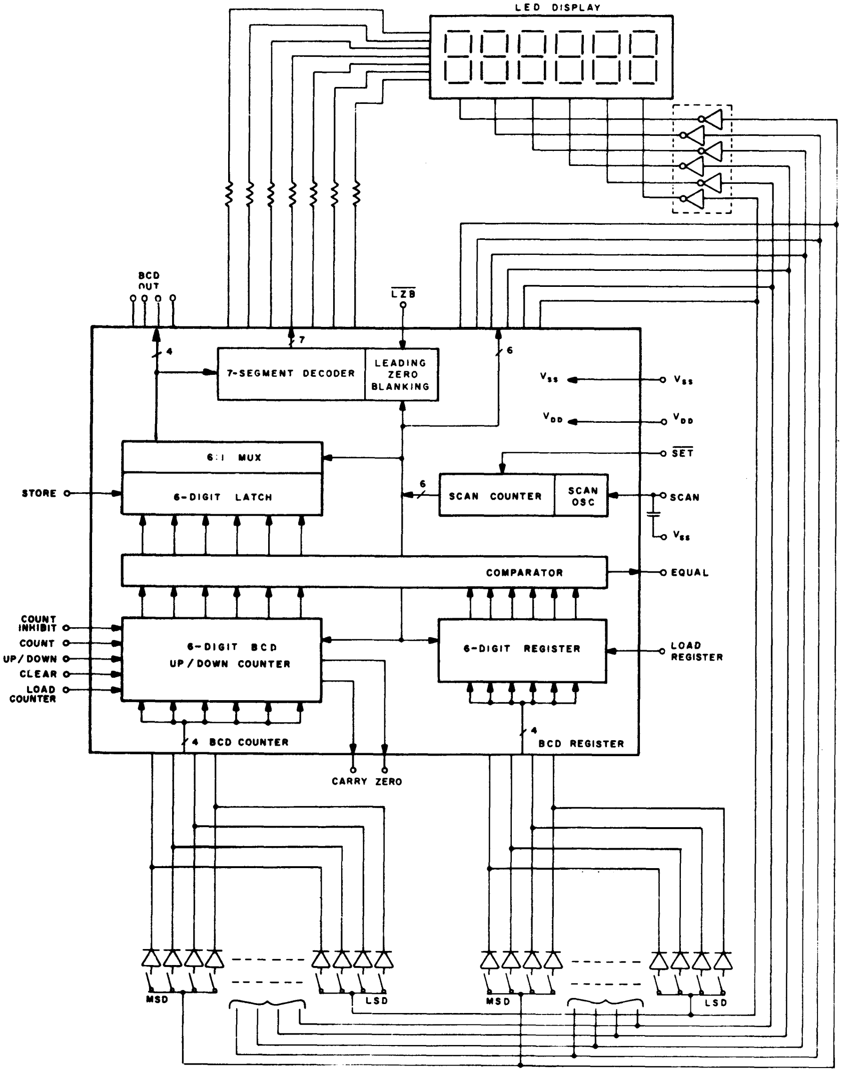
---

*Carry occurs at 99 59 59 for the MK 50396 and 59 59 99 for the MK 50397

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from Vss to the Scan input:

	Min	Max
820pF	1.4kHz	4.8kHz
470pF	2.0kHz	6.8kHz
120pF	7.0kHz	20kHz

FUNCTIONAL DIAGRAM
FIGURE 2



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS}. . . . . +0.3V to −20V
Operating Temperature Range (Ambient). . . . . 0° C to +70° C
Storage Temperature Range (Ambient). . . . . -40°C to +100°C

MAXIMUM OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply Voltage (V_{DD} = 0V)	10	15	V	
I_{SS}	Supply Current		30	mA	1
B_V	Break-Down Voltage (Segment only @ 10 μA)		$V_{SS} - 26$	V	
P_D	Power Dissipation		670	mW	2

ELECTRICAL CHARACTERISTICS

(V_{DD} = 0V, V_{SS} = + 10.0V to + 15.0V, 0°C $\leqslant T_A \leqslant$ 70°C)

Static Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Voltage, "0"	V_{DD}	20% of Vss	V	
V_{IH}	Input High Voltage, "1"	$V_{SS}-1$	V_{SS}	V	3
V_{OL}	Output Voltage "0" @ 30μ A		20% of Vss	V	4
V_{OH}	Output Voltage "1" @ 1.5 mA	80% of Vss		V	4
I_{OH}	Output Current "1" digit strobes segment outputs	 3.0 10.0		 mA mA	 5 6
I_{SCAN}	Scan Input Pullup Current @ 0V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15V	2	40	μ A	
$I_{\overline{SET}}$	$\overline{\text{SET}}$ Input Pullup Current @ 0V	5	60	μ A	

NOTES:

1. I_{SS} with inputs and outputs open at 0°C 28mA at 25°C and 25mA at 70°C. This does not include segment current. Total power per segment must be limited so as not to exceed power dissipation of package. (θ_{JA} = 100°C/Watt)
2. All outputs loaded.
3. MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS} -2.5V. Those inputs have internal pulldown resistors to V_{DD}.
4. This applies to the push-pull CMOS compatible outputs. Does not include digit strobes or segment outputs.
5. For V_{OUT} = V_{SS} -2.0 volts. Average value over one digit cycle.
6. For V_{OUT} = V_{SS} -3.0 volts. Average value over one digit cycle.

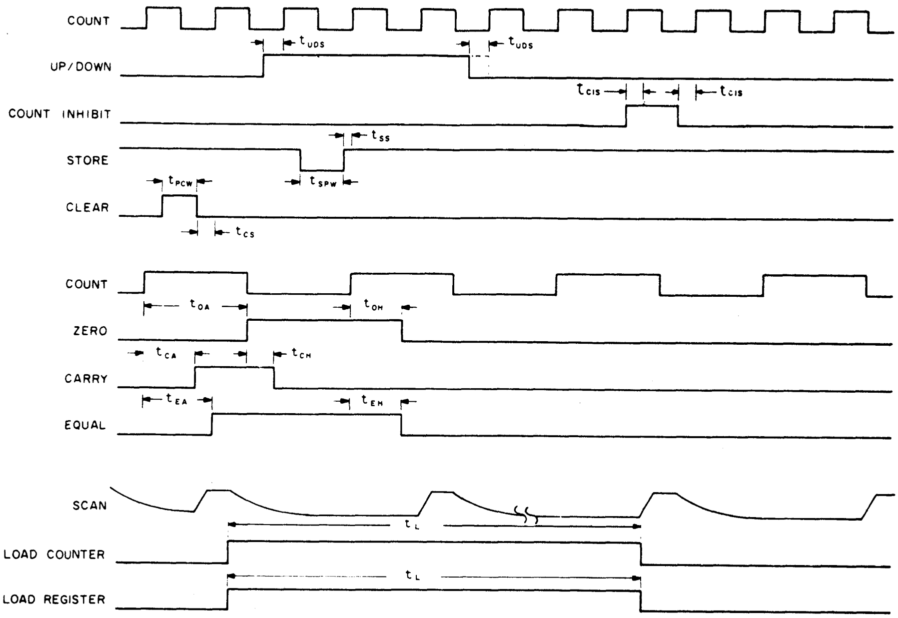
Dynamic Operating Conditions

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.00	MHz	7, 8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	400		ns	9
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Setup Time	0		μs	10
t_{CIS}	Count Inhibit Setup Time	0		μs	10
t_{UDS}	Up/Down Setup Time	- 0.75		μs	10
t_{CPW}	Clear Pulse Width	2.0		μs	10
t_{CS}	Clear Setup Time	- 0.5		μs	10
t_{OA}	Zero Access Time		3.0	μs	10
t_{OH}	Zero Hold Time		1.5	μs	10
t_{CA}	Carry Access Time		1.5	μs	10
t_{CH}	Carry Hold Time		0.9	μs	11
t_{EA}	Equal Access Time		2.0	μs	10
t_{EH}	Equal Hold Time		1.5	μs	10
t_L	Load Time	1/6 f_{SI}			

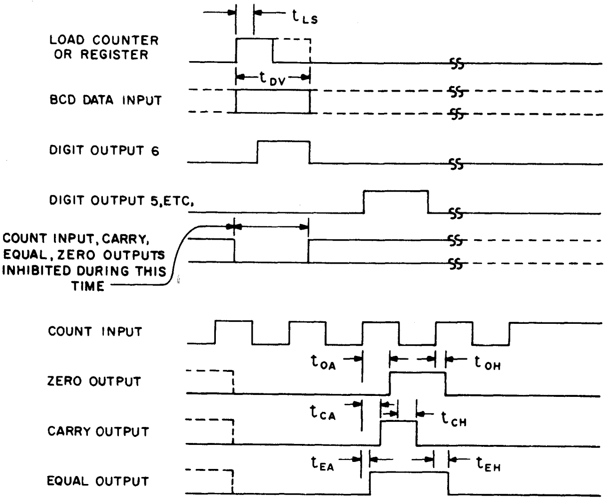
NOTES:

7. Measured at 50% duty cycle.
8. If Carry, Equal, or Zero outputs are used, the count frequency will be limited by their respective output times.
9. The count pulse width must be greater than the carry access time when using the carry output.
10. The positive edge of the count input is the t 0 reference.
11. Measured from negative edge of count input.

TIMING
FIGURE 3



LOADING COUNTER, REGISTER (1 DIGIT)
FIGURE 4



t_{LS} 2.0 µsec min NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 µsec min NOTE: REF TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:

The inhibit function of the Zero or Equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 µsec prior to a positive transition of a digit output. This same timing restriction hold for Equal and Load Register.

MOSTEK®

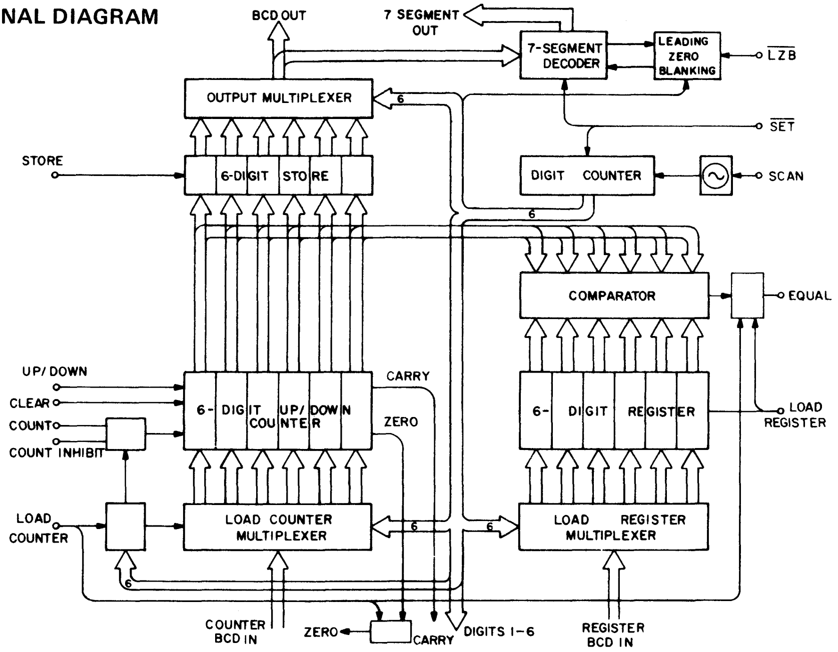
MK50395 SERIES COUNTERS

Application Note

MOSTEK'S SIX-DECADE COUNTER/DISPLAY TOTALIZER

Application Information Using Mostek's Six-Decade Counter/Display Totalizer

FUNCTIONAL DIAGRAM



The MOSTEK MK 50395 has been developed, after careful counter application analysis, as a counting system for most needs. The functional diagram shows that the system consists of six synchronous, up-down decade counters with a data store and an auxiliary storage register that may be compared with the counter value. The circuit is relatively insensitive to power supply variation, and can interface with CMOS logic using power supplies in the 10-to 15-volt range. Counting speeds up to 1.0 MHz are permissable and the circuits are readily cascaded.

Positive logic, i.e., logic 1 is the more positive level, is used in the following description:

THE COUNTER

The positive-going edges of a pulse train at the COUNT input (pin 36) are standardized by an internal monostable to a fixed pulse width, thereby giving only a minimum value to the time for which the input pulse must stay high. This pulse is applied synchronously to the six decades and, if the UP/DOWN input is a logic 1, the counters will be incremented. If at logic 0, then the counters will be decremented. At any time, the value in the counter will be set back to zero if the CLEAR COUNTER input goes to a logic 1 for 2 μs or longer. This resetting action occurs whether or not there is a counting input pulse train.

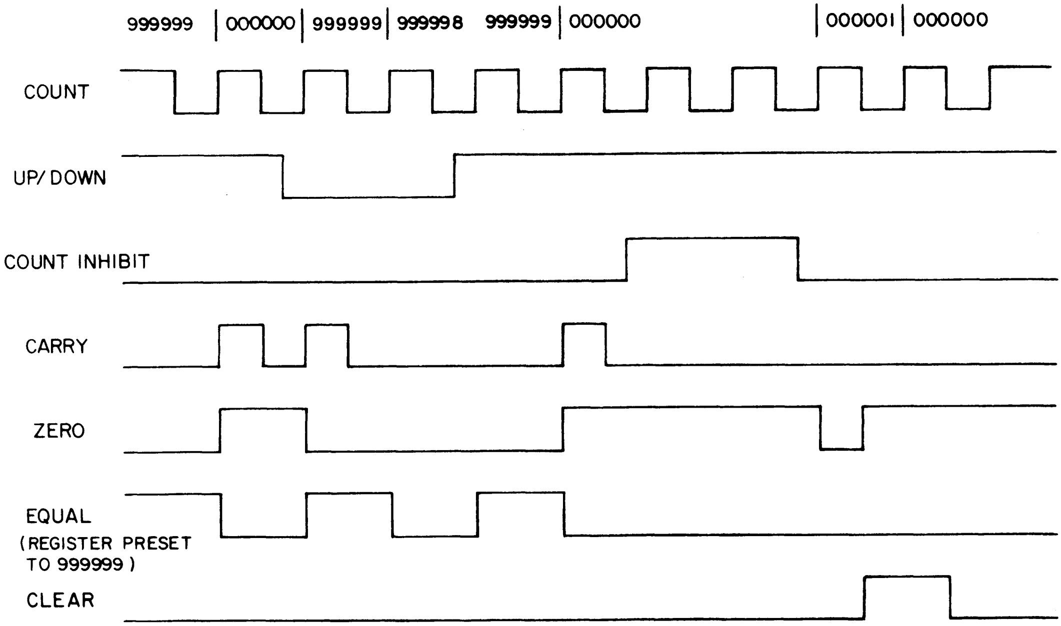
In addition to resetting, it is also possible to preset any desired value into the counter. This is done sequentially, decade-by-decade, under control of the LOAD COUNTER command, in the following manner. If LOAD COUNTER is taken to logic 1 a minimum of 2 microseconds prior to the positive transition of the digit output of the digit being loaded, the chip will latch this command and the BCD data presented to the counter will be loaded on the negative transition of the digit strobe. It is thus possible to load each of the 6 counters individually, if required. While the counter is being loaded, the counting input is inhibited. Internally, the load counter command is synchronized to the scan oscillator. Thus, if load counter is brought to a logic zero in the middle of a digit strobe, the counter will remain inhibited until the next interdigit blanking time. A separate COUNT INHIBIT control is provided to stop the applied count inputs from being accepted while this signal is a logic 1.

The counter section has two control outputs, a CARRY from the most significant decade and a ZERO SIGNAL that indicates when the counter contents are zero. These signals are suppressed during LOAD COUNTER operations to avoid a spurious output being given during a counter presetting operation.

COMPARISON AND REGISTER

The six-digit storage register may be preset to any value by bringing the LOAD REGISTER signal to logic 1. The presetting sequence is exactly the same

UP/DOWN COUNT TIMING

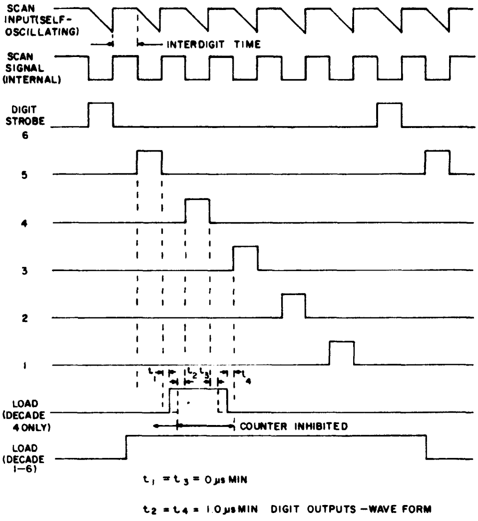


as for the counter. The value on the REGISTER BCD INPUTS is loaded decade-by-decade by the six digit signals in the order "most significant" (digit 6) to "least significant" (digit 1). The outputs of this register are compared continuously with the value currently in the counter. This comparison is made in parallel and not decade-by-decade. When the two values are the same, an EQUAL signal is given. However, during presetting of the counter the CARRY, ZERO and EQUAL signals are inhibited so that no false, intermediate comparison result is given. Since the counter and the register have separate BCD inputs, both may be preset simultaneously if desired. The value held in the register can only be altered by the BCD inputs. The Count Input is not inhibited during load register operations.

DIGIT SCANNING AND OUTPUT FUNCTIONS

The digit scan counter is timed from an internal oscillator which may be driven externally from the SCAN input. A capacitor attached from V_{SS} to this pin will determine the scan frequency when external logic drive to this pin is not used. Intenal circuitry gives a fixed delay to the DIGIT OUTPUT signal to ensure that there is a gap between each digit strobe so that a "ghosting" effect in a displayed output due to the storage time of external display driver transistors is eliminated. This is the interdigit blanking time. Typically, this time can range from 3 to 10 microseconds.

LOAD COUNTER, REGISTER TIMING



the $\overline{SET}$ input is used to force the digit strobe counter to the digit 6 position for purposes of synchronizing the counter output. The digit counter outputs are gated by the interdigit blanking period and appear as DIGIT STROBE OUTPUTS. The counter outputs are not directly multiplexed but are buffered by a 6-digit latch controlled by the STORE command. The out-puts of the latch go directly to the output multiplexer. Thus, when the STORE signal is at logic 0, the counter contents are directly available, but as soon as STORE goes to logic 1, the value present as the signal changed is retained and subsequent changes in counter value are ignored. The contents of the store are read out, digit-by-digit — the scan counter again performs this function in the order most-significant to least-significant — and appear on BCD OUT pins. The four bits in each BCD digit are encoded simultaneously to seven-segment code and appear as SEGMENTS OUT and can be used to drive a suitable 7-segment display. The SET operation will also turn off these seven outputs, blanking the display, as well as setting the digit counter to digit 6. This is to prevent possible destruction of an LED-type display when SET is a prolonged signal. Frequently it is required to display only significant numbers, in which case taking the $\overline{LZB}$ control to a logic 0 will blank the leading zeros in the seven-segment output.

INTERFACING WITH THE MK 50395

The wide range of power supply, 10.0 – 15.0 volts, makes the counting system particularly suitable for interfacing with CMOS logic.

A. Segment output — these transistors can source 10 mA from the Vss supply. There is no internal pull-down to VDD when the transistor is turned off. These transistors are capable of driving small LED displays directly via series resistors.

B. Digit outputs – a push-pull configuration is used here as the most suitable arrangement for driving both external logic and display drivers. These outputs supply 3.0 mA max from V_{SS} and sink 30 μA to V_{DD}.

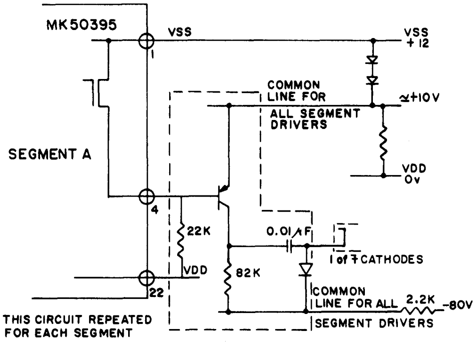
When higher-power displays are used, the segment outputs should be buffered by an emitter follower in order to provide the extra current.

The BCD OUTPUTS, EQUAL, ZERO and CARRY are also push-pull. Output drive capabilities are listed in the following table:

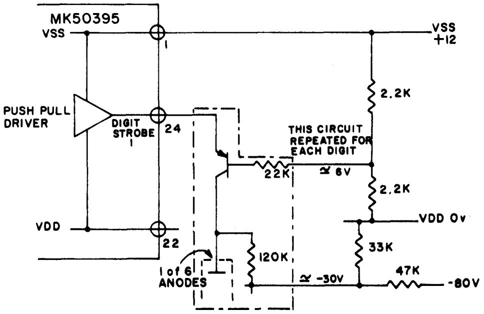
	VOL	VOH
Segment Output (Pins 4-10)		V_{SS}–3V at 10mA (average over one digit strobe cycle)
Digit Outputs (Pins 24-29)	VDD at no load 20% of Vss at 30 μA	V_{SS}–2V at 3.0mA
Equal/Zero/Carry (Pins 23,39,38)	VDD at no load 20% of Vss at 30 μA	V_{SS} –2V at 1.5mA

The following inputs, COUNT, STORE, UP/DOWN, COUNT INHIBIT, CLEAR, $\overline{LZB}$, LOAD REGISTER have no internal current sources and must therefore be driven from sources that give correct logic 1 and 0

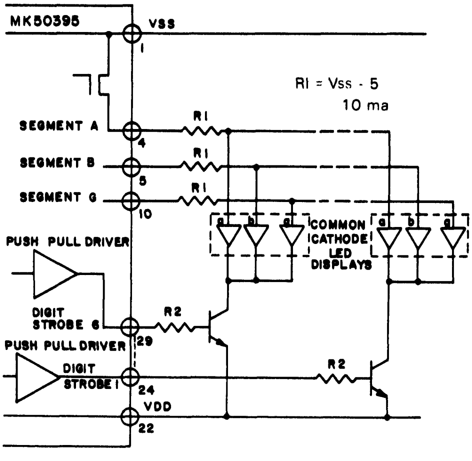
SEGMENT DRIVER



DIGIT DRIVER



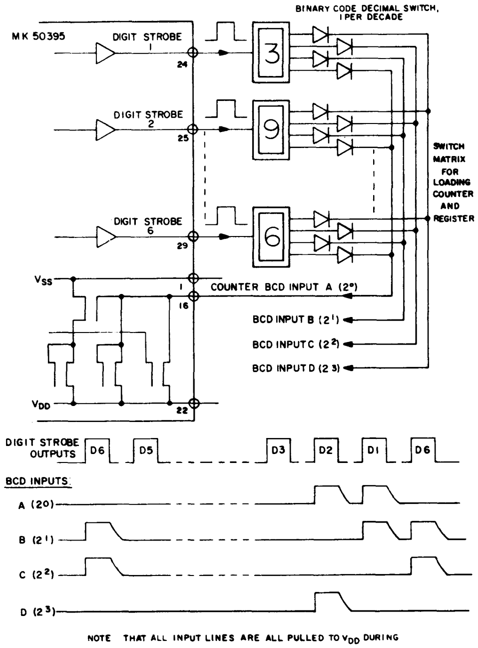
DRIVING LED DISPLAYS DIRECTLY



levels - open collector circuits, or switches without pull down resistors for example, may not be used. If any of the above functions are not required then those pins should be tied to the appropriate supply, that is to V_{SS} for logic 1 and V_{DD} for logic 0. $\overline{\text{SET}}$ has an internal transistor that pulls the pin to V_{SS} if unconnected thus the driving circuit should be able to sink this current, approximately 60 μA, when pulling the input to logic 0. The COUNTER BCD and REGISTER BCD inputs have two internal transistors one static and one switched as a precharge, that pull to V_{DD}. The static current is < 350 μA to V_{DD} when the input is taken to V_{SS}, the dynamic current from V_{SS} is 1 mA while the transistor is on. The dynamic precharge ensures that even with the large capacitive loading and leakage current of a switch matrix at these pins, the correct data will be entered at the maximum digit scan frequency.

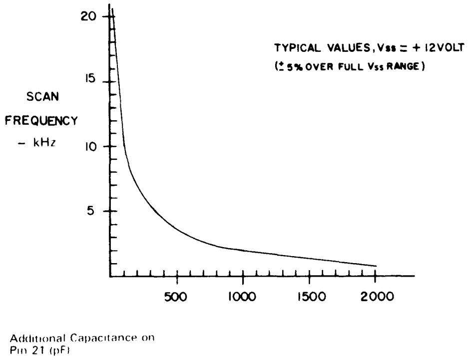
An example of a switch matrix input illustrates this operation. Six binary-coded-decimal switches are used, one for each decade, the switches being enabled by the corresponding DIGIT STROBE output, with the paralleled switch outputs connected to the COUNTER (or REGISTER) BCD inputs. The DIGIT STROBE outputs are separated by the interdigit blanking time and it is only during this time that the precharge transistors at the BCD inputs are all pulled to logic 0 (V_{DD}). After this blanking time, the next DIGIT STROBE output will in its turn switch to logic 1 (only one out of six is ever on) and pull those BCD inputs selected by the switch and diode matrix to logic 1. This value is loaded into the corresponding register or counter stage, i.e. the switch matrix driven by DIGIT STROBE 6 will be loaded into MSD of the register or counter. As the DIGIT STROBE switches back to logic 0, the next interdigit blanking time begins and the inputs are all pulled back to logic 0 again by the internal precharge. It is possible for the DIGIT STROBE outputs to drive both the switch matrix and a display. If the COUNTER & REGISTER BCD inputs are connected in parallel they may still be driven directly from the DIGIT STROBE outputs.

BCD SWITCH MATRIX



NOTE THAT ALL INPUT LINES ARE ALL PULLED TO V_{DD} DURING INTERDIGIT BLANKING

SCAN FREQUENCY VS EXTERNAL CAPACITANCE



When the scan oscillator is free running, the SCAN input may use an external capacitor to set the scanning frequency to a particular value. The signal seen at the pin is a ramp determined by the capacitance, followed by a period clamped at V_{SS}. This period clamped at V_{SS} is determined by the internal oscillator and is the interdigit blanking period. During this time, the DIGIT STROBE outputs are all turned off. When the SCAN input is driven externally, this fixed interdigit period remains plus the time at which the synchronizing signal is at logic 0. To make the interdigit blanking time independent of the external synchronizing signal requires only the addition of a resistor and capacitor as shown on page 50.

Referring to the External Drive To Scan Input drawing on page 50, time a is the interdigit blanking time.

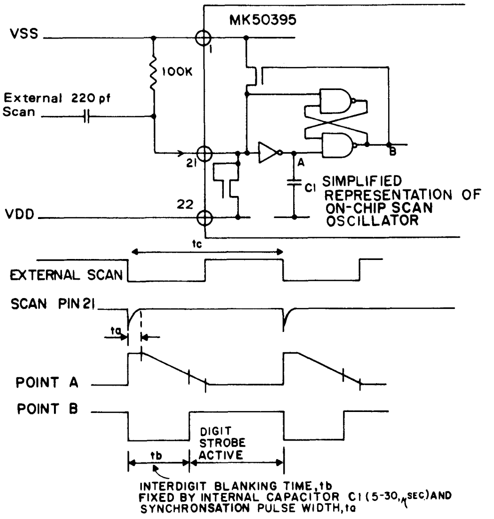
Time b should be greater than 2μs—a range of 2–5μs is suitable-and time c may be from infinity to 30μs. If time c is made too short, then the interdigit blanking circuit never resets itself and will stay at logic 0 and no DIGIT STROBE outputs will appear.

TYPICAL MK 50395 APPLICATIONS

BATCH CONTROL

In many situations involving the metering of material, whether as a liquid, individual items or revolutions of a spindle, a two-step operation is required for better efficiency. The flow is started at the maximum speed and at a preset point before the end of the operation a signal is required to slow down and eventually stop the equipment. Such applications could be as diverse as filling sacks with cement or controlling the turns on a transformer bobbin. In the system shown on page 50, pressing the start switch allows the input to the D flip-flop to go to logic 1. This is clocked by DIGIT STROBE 6 so that a synchronous signal at least one complete scan counter cycle

EXTERNAL DRIVE TO SCAN INPUT



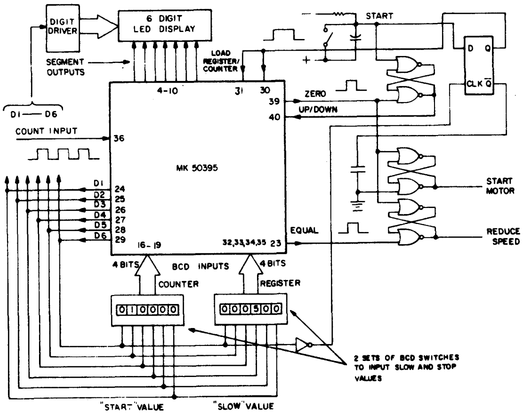
long is obtained. This signal is used as LOAD COUNTER and LOAD REGISTER, the two controls being tied in parallel for simultaneous loading. It does not matter how long the load signal is so long as it is at least one scan cycle long and changes synchronously with the scan signal. The two values representing total quantity and "slow-down" quantity are set on the digit switches and these values are loaded at the beginning of each cycle. Once the counter register loading is complete, a start signal is generated to set the equipment in operation. While the train of pulses representing the measured quantity is counted, the UP/DOWN control is in the down mode. Thus with two quantities at, let us say, 10,000 and 500 the counter starts off with 10,000 loaded and counts toward zero. When the counter reaches 500, an EQUAL signal is generated and this sets the signal controlling the brake. After a further 500 pulses, the counter reaches zero, an output on the ZERO pin resets the start flip flop and the equipment is brought to reset awaiting a new start signal. In such an operation the display outputs would probably not be used.

This application can be extended by using the ZERO output to control the UP/DOWN input. The operation is identical but the start signal also sets a latch into the count down state. As ZERO is detected this latch is reset so that the counter mode is now up. Even with a braking facility there may be an "overrun" and the value now held in the counter and displayed is the extra quantity. The operator may now decide if this extra quantity is within the tolerance allowed for the job and to take whatever action is necessary.

POSITIONAL MEASUREMENT

Positional measurement can readily be made using this circuit. The six decades gives considerable ac-

BATCH CONTROL



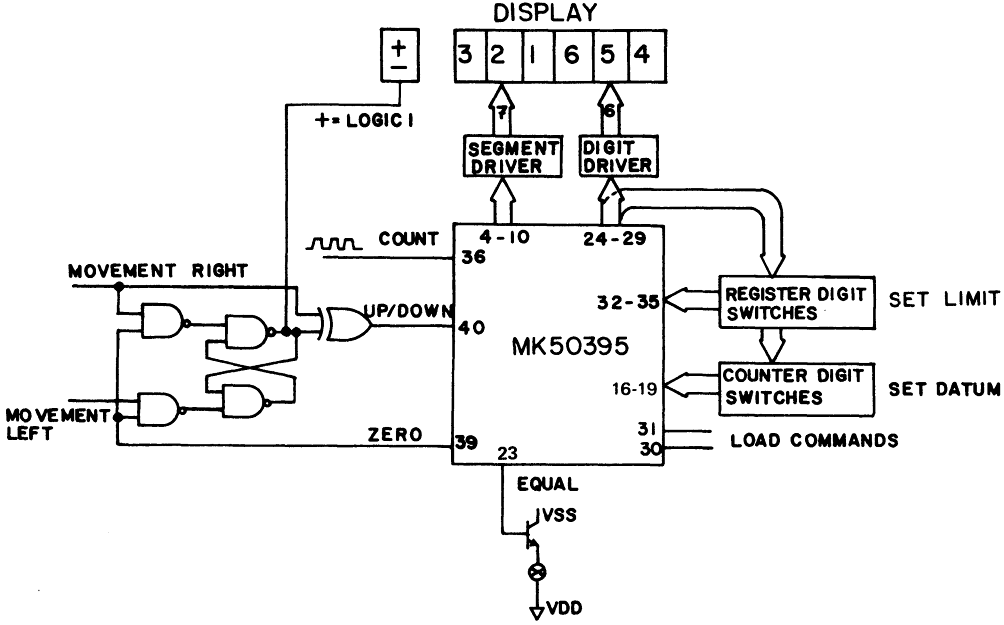
curacy in one package. The two quadrature signals from a graticule-type displacement measurement system must be converted to count impulses and an UP/DOWN signal. If the measurement zero datum is in the middle of the measurement area then the following counting conditions arise:

Direction of Movement	Displayed sign + or − of Datum	Count direction	
RIGHT	−	DOWN	ZERO DATUM CROSSED
RIGHT	+	UP	
LEFT	+	DOWN	ZERO DATUM CROSSED
LEFT	−	UP	

Each time the zero datum is reached and each time the direction of movement is changed, the count direction must be changed. The value displayed thus represents the position either side of the zero datum. The storage register may be used as a means of limiting the travel of the measurement piece. If a value equal to the limit is loaded into the register, the EQUAL output may be used to give a warning that the limit is reached.

It will have been noted from the delay of EQUAL and ZERO to the COUNT edge that ZERO has much longer propagation delay than the EQUAL output. In the event that the register is not used, it may be loaded with zeros — by giving a LOAD REGISTER command with the BCD inputs as zero — and the EQUAL output then used as zero detect. This has the advantage of increasing the system speed, for, although the counter can accept inputs up to 1.0 MHz, the propagation delay of the outputs is too long to allow a control signal to be changed between clock pulses at this counting rate. In this example, UP/DOWN has to be controlled, and using the faster out-

POSITIONAL MEASUREMENT



put enables a higher counting speed, 600 kHz instead of 300 kHz, to be used if necessary.

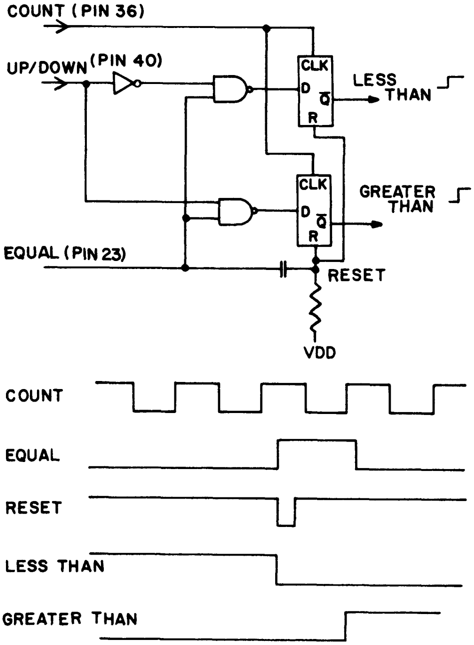
GREATER THAN – LESS THAN DETECTION

The availability of an EQUAL output facilitates the generation of greater-than and less-than signals. The only requirement is that the circuit is set into the correct initial state. When the counter has the same value as the register, the generation of the "greater/less than" signal depends on the direction of count, i.e. from this EQUAL condition count up gives "greater than" and count down gives "less than". EQUAL is gated with UP and with DOWN and these are connected to the D inputs of two D flip-flops that are both clocked by the counting pulse. As EQUAL is reached, the two flip flops are reset but the next count pulse after the EQUAL condition will set one of the flip flops and thereby provide the appropriate signal.

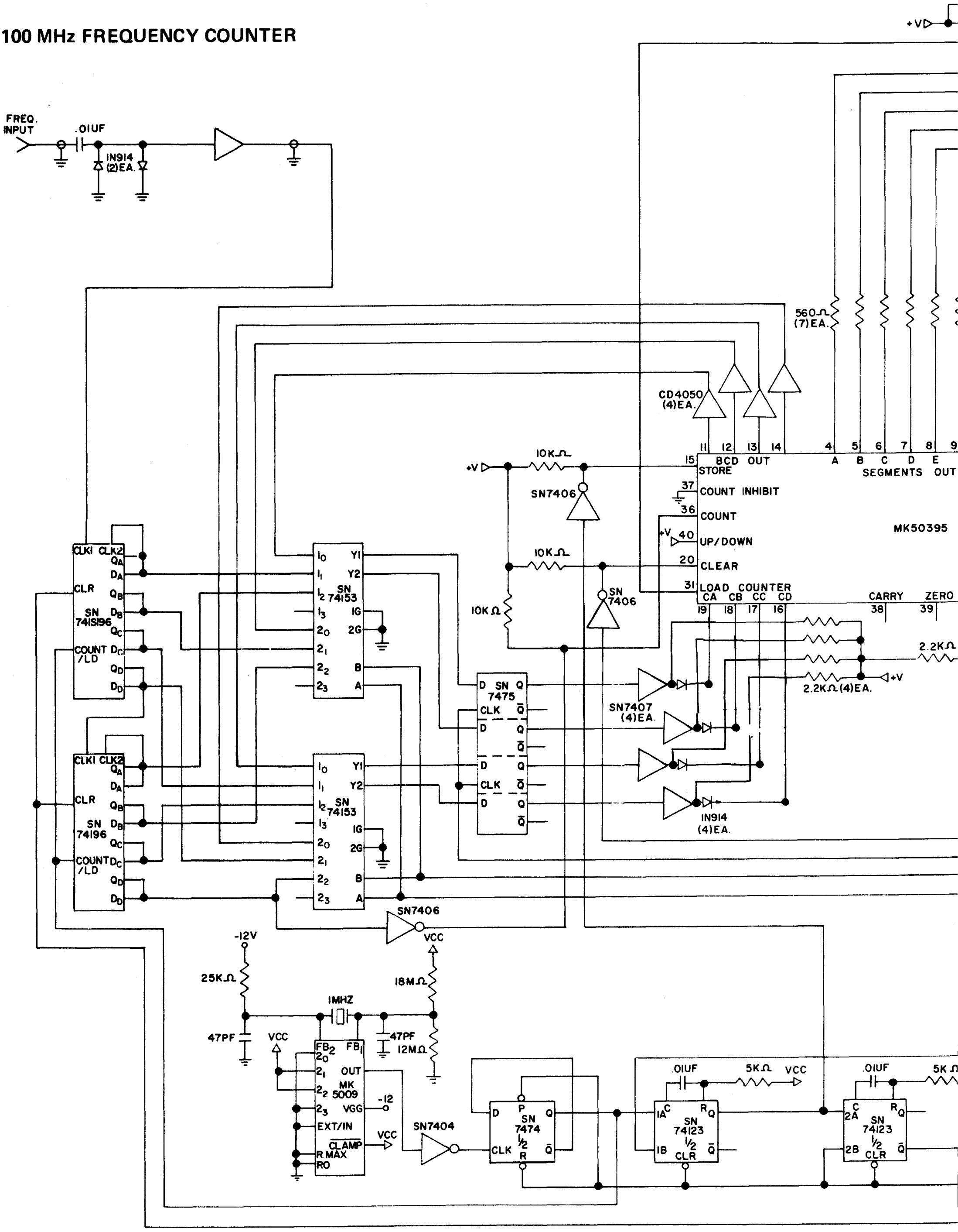
AUTOMATIC STOP

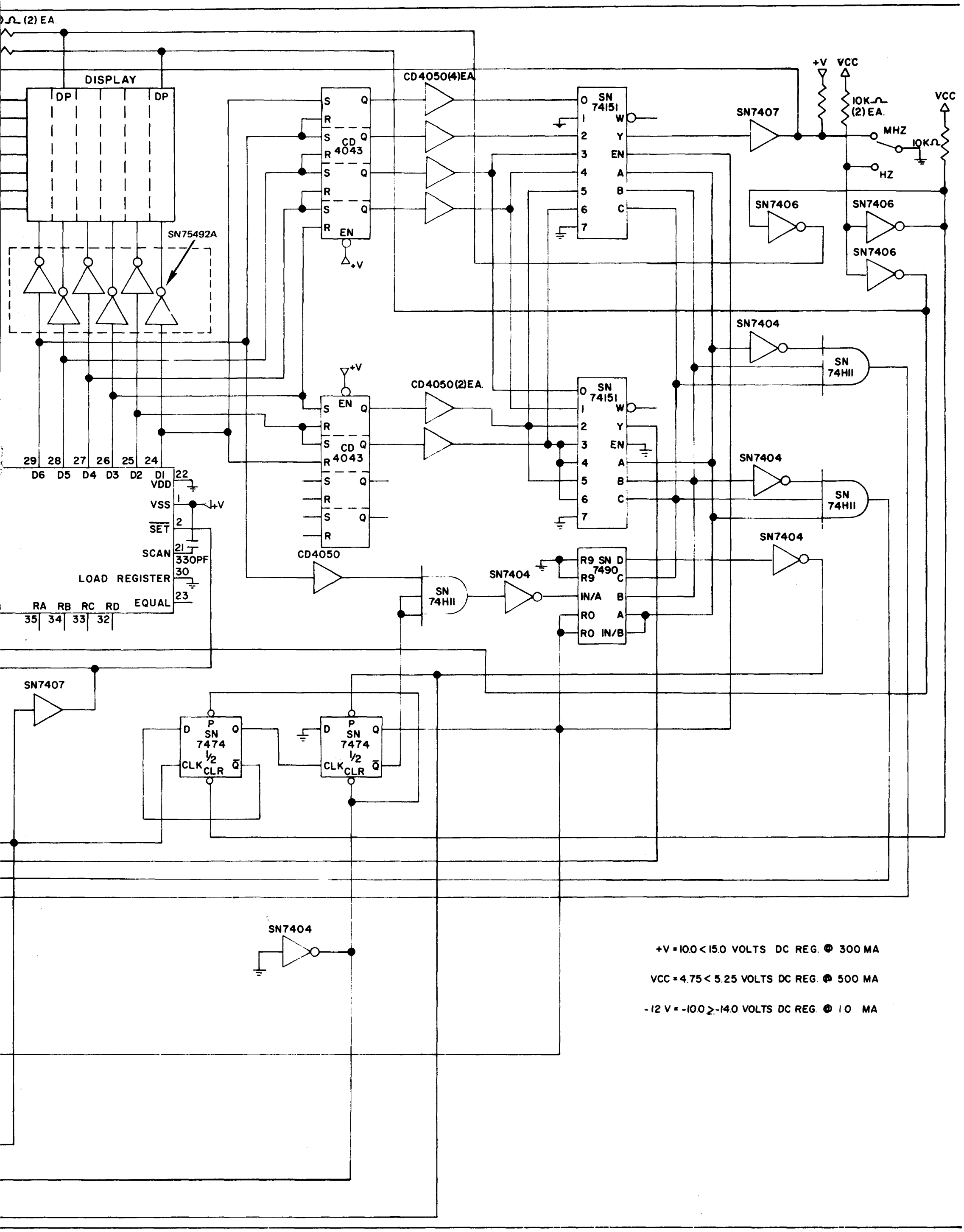
The COUNT INHIBIT input may be used to stop the counter automatically when the EQUAL or ZERO outputs are connected directly to this input. As EQUAL, for example, goes to a logic 1, then further counting is inhibited when this signal is connected directly to COUNT INHIBIT. Since no more count inputs are accepted, the EQUAL value remains and blocks the counting action. The operation of CLEAR, LOAD REGISTER or LOAD COUNTER can be used to start the system counting again.

GREATER THAN — LESS THAN



100 MHz FREQUENCY COUNTER



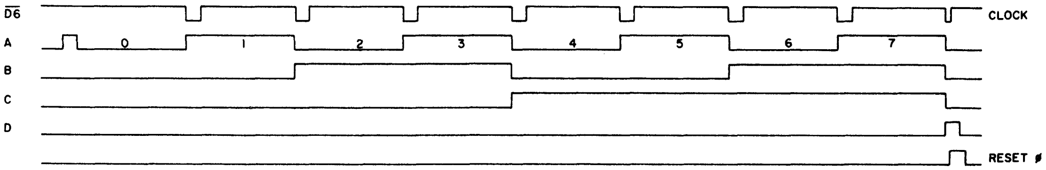


+V = 10.0 < 15.0 VOLTS DC REG. @ 300 MA

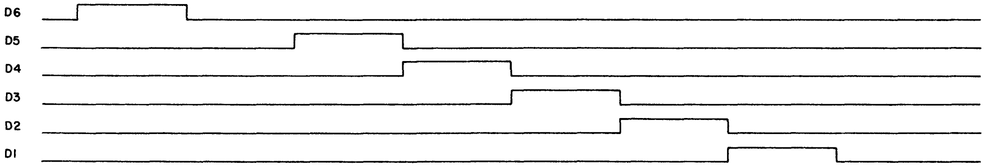
VCC = 4.75 < 5.25 VOLTS DC REG. @ 500 MA

-12 V = -10.0 ≥ -14.0 VOLTS DC REG. @ 10 MA

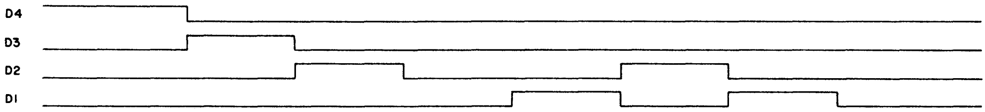
SN 7490 TIMING



SN 74151 LOAD COUNTER PULSE TRAIN OUTPUT



SN 74151 OUTPUT TO BCD LATCH ENABLE



SN74153's DECODE
$A = \bar{A} \cdot B \cdot C$ $B = A \cdot \bar{B} \cdot C$

MORE APPLICATIONS

The following applications resulted from an ad contest sponsored by Mostek. These applications represent a cross section of uses for the MK 50395 family and are intended as a guide for applying the counter circuit.

The type of display is left to the user to design into his particular application. The MK 50395 series was designed to allow direct drive of efficient display systems. If the current requirements of a display exceed the specifications of the MK 50395 series, external segment drive circuitry will be required.

Power supply voltage range, wattage, filtering, and decoupling must be observed in all applications. The MK 50395 series was designed to keep power supply restrictions to a minimum.

100 MHz FREQUENCY COUNTER

In most counter applications, the problems associated with prescaling result in a loss of resolution, or the need for longer count sample times. This application allows the MK 50395 with some associated circuitry to count at 100 MHz with a one-second gate time achieving one-Hz resolution.

The MK 50395 counts the input frequency after a divide-by-100 using an SN74S196 and an SN74196. Frequency sample time is achieved by a one MHz crystal in conjunction with the MK 5009 time base in the ÷ 10^6 configuration, followed by a divide-by-two to give a one-second logic one level. This is applied to the count/load input of the SN74S196 and SN74196 counters. The 10's-of-Hz and one's-of-Hz data is retained in these two counters for later display. Actually, only a count of 99.9999 MHz may be displayed as the MK 50395 would display all zeros and a carry would be generated at the next higher count.

At the end of the one-second sample time, a store is generated and the count data is latched into the display.

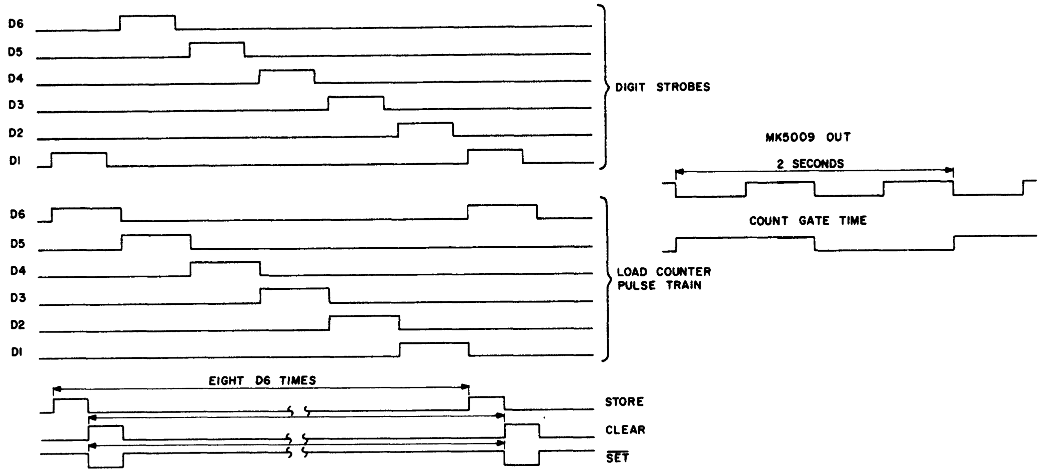
A clear counter pulse is generated to ready the MK 50395 for the next data cycle. If the MHz-Hz switch is in the MHz position, the preceeding cycle will again occur at the next gate sample time. Load counter is also disabled in the MHz position.

With the MHz-Hz switch in the Hz position, the first ½ SN7474 is enabled and is clocked at the end of every pulse, which clears the MK 50395. The second SN7474 also changes state, enabling the SN74151 which controls the MK 50395 load counter input, and the Hz cycle begins.

At the end of every clear MK 50395 pulse, $\overline{\text{SET}}$ is brought low to sync the MK 50395 with the rest of the circuitry.

The MK 50395 loads digit Six with digit Four data into the BCD counter. The digit four data was stored in the SN7475 latch at the previous digit four time.

TIMING DIAGRAM



The SN7490 is advanced one count at the digit six time at the start of the sequence.

Latch Digit Four Data,
Load Into Counter Digit Six

Latch Digit Three Data,
Load Into Counter Digit Five

Latch Digit Two Data,
Load Into Counter Digit Four

Latch Digit One Data,
Load Into Counter Digit Three

At this time, the output of the SN7490 is decoded to select via the SN74153's first digit two data, then digit one data is selected which at the end of sample time was stored in the SN74196 and SN74S196. So the sequence is continued.

Latch Digit Two Data
Load Into Counter Digit Two

Latch Digit One Data
Load Into Counter Digit One

At the beginning of the eight count of the SN7490 several things take place. The MK 50395 is furnished with a store pulse to display the shifted data. A clear is applied to the MK 50395 to ready it for a new cycle.

The divide-by-two action of the first ½ SN7474 allows the second clear clock to have no effect at the second clear pulse. The SN74S196 and SN74196 are cleared. The second ½ SN7474 is preset which disables the load counter SN74151. The SN7490 is reset to zero.

To improve front end sensitivity, a suitable wideband amplifier may be used. A typical device would be a μA 733. Timing diagrams for the MK 50395 and the associated circuitry are provided to further describe the various functions.

DARKROOM TIMER – A TYPICAL APPLICATION

A darkroom timer capable of being set for time periods from 99 minutes and 59 seconds is illustrated. The time interval to be set is entered into the BCD thumbwheel switches. Upon pressing the start button, the time indicated on the thumbwheel switches causes the counter to be loaded identically. Diode CR1 loads the register for a prewarning signal (8 seconds in diagram) prior to the end of the time interval so the operator can be alerted to the fact that the time interval is about over.

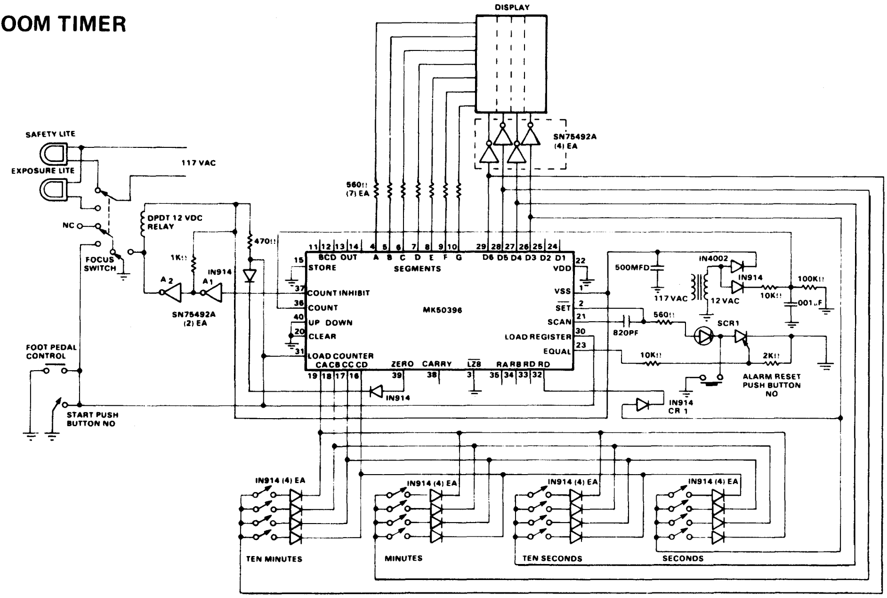
Resistor network R_1, R_2 lowers the 60Hz line voltage so that the positive peak does not exceed Vss. Otherwise, damage to the circuit could occur. The counter input is driven directly from the 60 Hz line frequency and the two LSD's are not monitored by the display since they perform a divide function in this application. The LED display will present the time remaining, since the counter is in the count down mode. If an illegal entry is made, such as binary 12, (1100), the display will show "E" in the digits containing an illegal entry. The counter will eventually "count out" the "E", but, of course, the time interval will not be useful. Also, it is possible to load illegal time such as 75 seconds. This illegal time will result in an error in timing.

Sequence of Events

Assume a time interval of 1 minute, 45 seconds has been selected and programmed into the thumbwheel switches.

1. Pressing the start button completes loading 1 minute 45 seconds into the counter. The register is loaded with the eight-second prewarning signal. The relay is activated, which allows the count down sequence to begin. (The display will imme-

DARK ROOM TIMER



diately show 1:44, because the — 60 stage will be counting down the 60Hz input.) The relay also turns off the safety light and turns on the exposure light.

2. When eight seconds to time-out occurs, the equal output goes to V_{SS} momentarily, turning on SCR_1, which lights an LED warning light that indicates the time interval is about over.

3. When the counter hits zero time, the zero output inhibits any further count input. The zero output also provides bias to turn on amplifier A_1 to turn off relay driver amplifier A_2, so the safety light will come on as the exposure light turns off.

4. The reset switch is used to turn off the SCR for the next time sequence.

DIGITAL TUNING INDICATOR

The MK 50395 is used to count and display frequencies of the FM frequency bands.

The frequency being sampled is buffered to TTL logic levels, then divided by 100 with an SN74S112 JK flip-flop, an SN74S196 and an SN7490. Transistor Q_1 then shifts the TTL logic levels to MOS logic levels.

The CMOS RC time base is adjusted to oscillate at 1kHz and is then divided by two to produce the necessary 500Hz time base.

At the end of the count sample time, a store is generated to latch the data into the display.

The placement of the diodes which determine the value to be loaded in the MK 50395 counter is dependent on the frequency of the local oscillator and whether high-side or low-side injection is used in the receiver.

In a typical FM receiver with High-side injection, a dial setting of 88.7 MHz means the local oscillator output would be 99.4MHz. To offset the 10.7MHz (88.7 + 10.7), the counter would be preloaded to 999893 (000000 minus 107). This effectively subtracts the 10.7MHz thus displaying the dial frequency. After each sample time, the MK 50395 counter is reloaded, readying it for the next count cycle. For low-side injection receivers, the preset would be 107 (00000 plus 107). This effectively adds 10.7MHz to the count. The decimal point of Digit two may be wired to +V through a resistor to produce the decimal in the FM mode.

To calibrate the time base, an oscilloscope or frequency counter may be used. However, careful adjustment at the low and high end of the counter display would be sufficient.

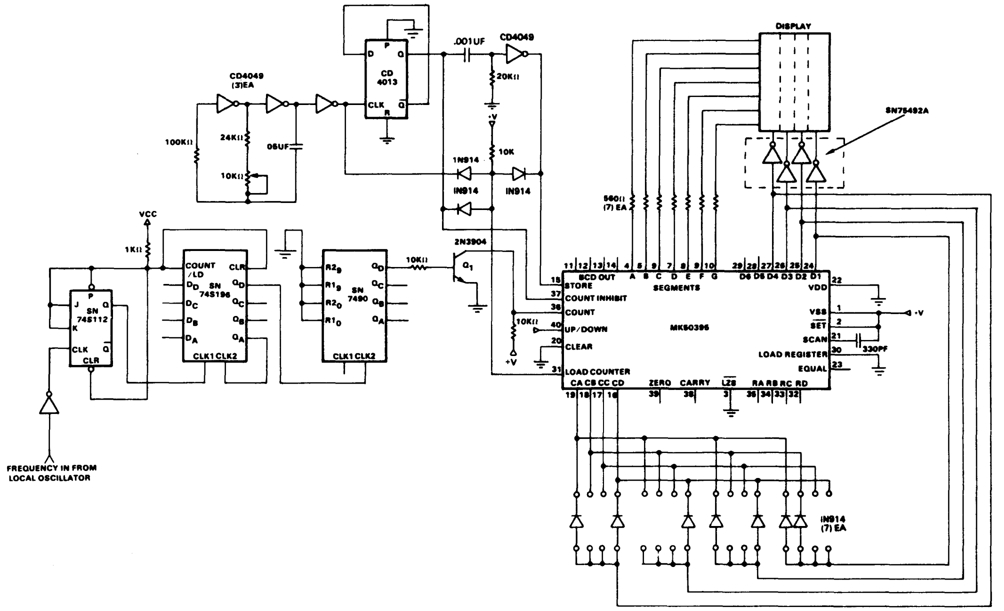
N PULSER

The N Pulser was designed to gate a specific number of pulses. Its design uses a minimum of external circuitry.

The number of pulses to be gated are entered into the thumbwheel switches. This value is loaded into the BCD Register with the LOAD button. When the MK 50395 counter reaches this value, the MK 50395 EQUAL output goes high. The pulse string is then interrupted.

To control frequencies above 500kHz, a suitable prescaler could be used at the MK 50395 count input, and compensated by the value entered into

DIGITAL TUNING INDICATOR

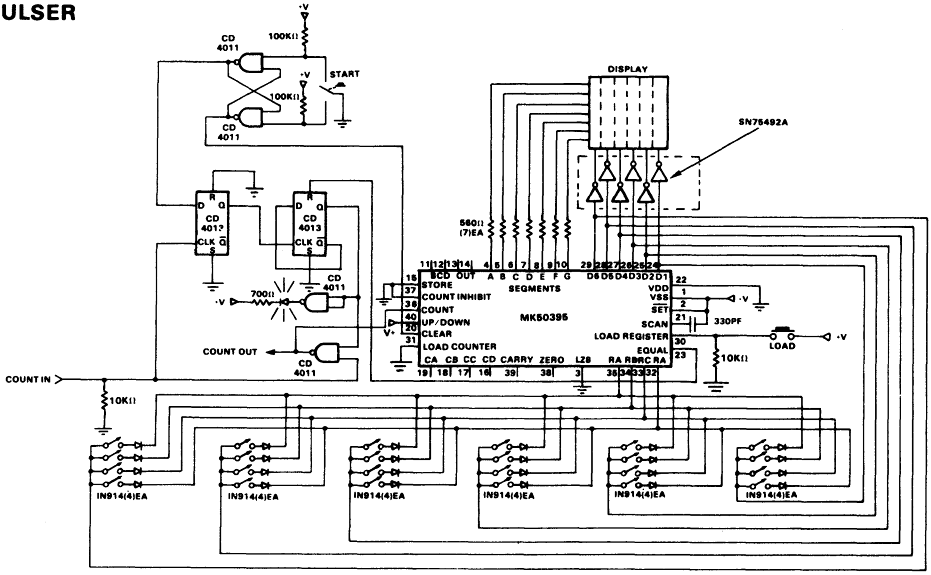


the MK50395 BCD Register. Pulses in and pulses out must be CMOS compatible, or suitable level shifters will be required.

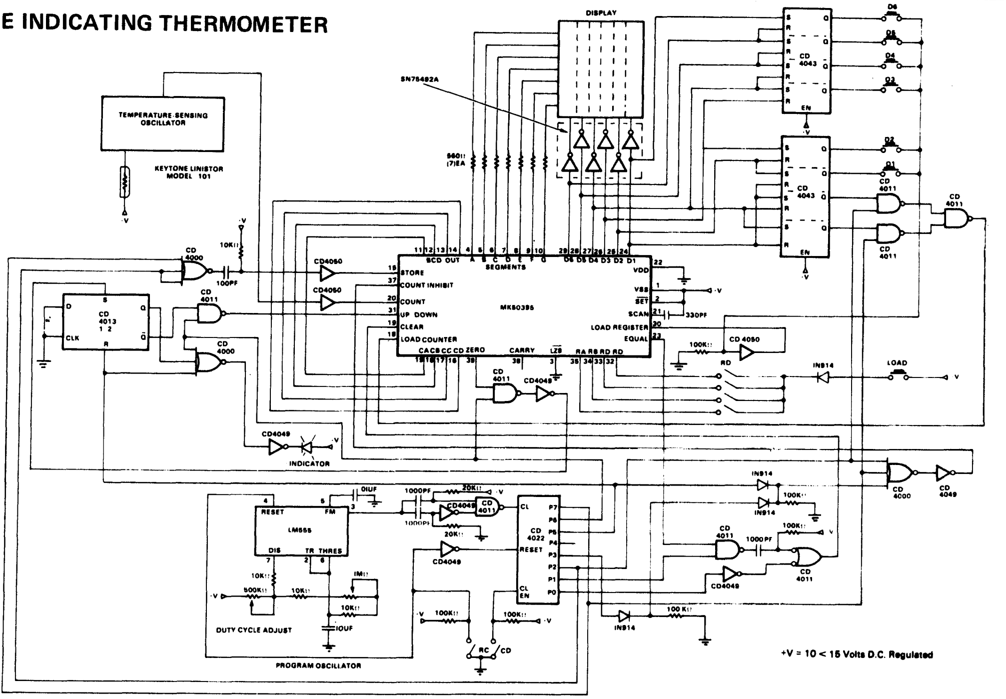
CONTINUOUS RATE-INDICATING THERMOMETER

The MK50395 displays the result of a program of eight periods (P0 through P7) under control of a

N PULSER



RATE INDICATING THERMOMETER



program counter (CD4022) which is driven by a program oscillator having independent controls for its frequency and its duty cycle. The output of the program oscillator is differentiated to supply a clock pulse to the program counter for each half cycle of the program oscillator. The program counter has eight decoded outputs which are used to time the program periods P0 through P7.

A voltage-controlled oscillator in conjunction with a thermistor converts temperature into frequency. After the initial calibration, it is desireable that the VCO be stable to maintain accuracy of temperature change indications, which occur during P4 and P6 times.

During P0, the P0 output of the program counter is high and the counter of the MK 50395 is reset. During P1, the MK 50395 counter is incremented at the rate of the pulses furnished by the temperature-sensitive oscillator. When the counter reaches equality with the register, the counter is reset to zero and continues counting until the end of P1.

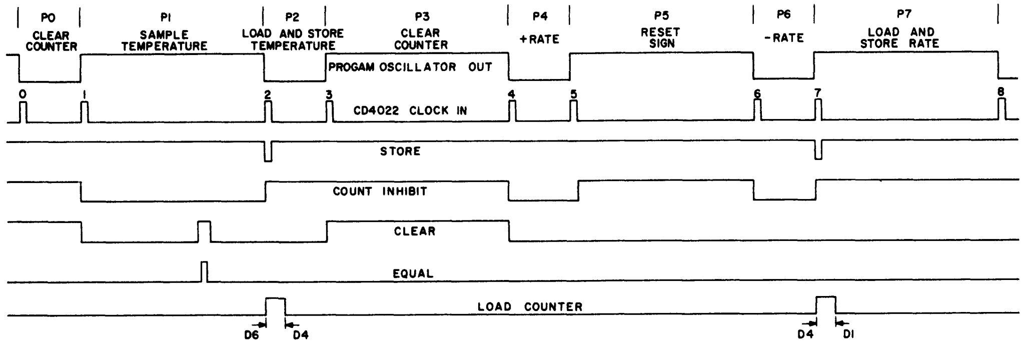
The length of the positive-going half-cycles of the program oscillator (during P1, P3, P5 and P7) is selected so that during the period P1, the number of cycles of the temperature-sensitive oscillator (which are counted) changes with temperature at the rate of one thousand cycles per degree (either F or C). For example, if the frequency of the temperature-sensitive oscillator is 75kHz at 70°F and changes at the rate of 1000 Hz per degree change of temperature, the positive-going half-cycle of the program oscillator is selected to equal 1.0 second vary the count of the 50395 counter (at the end of P1) by 1000 counts per degree. The register is preloaded with a quantity to calibrate temperature. In the the above example, the register is preloaded with the quantity 80,000 so that the counter stands at 70,000 (150,000–80,000) at the end of P1 indicating a temperature of 70°F. Only the three most significant digits of the MK 50395 counter are displayed for temperature, and the display indicates the temperature in degrees, 70, 71, etc. The leading zero is blanked.

The three most significant digits of the counter indication are set into the MK 50395 latch during P2, but not before the three least significant digits of the counter are loaded to a quantity equal to that stored in the three least significant digits stored in the latch. These counter digits are set by bringing the load counter pin 31 high at the end of digit 4 thru digit 1 time and then bringing the store pin 15 low after the leading edge of D3, D2, and D1 with a delay. The four BCD output pins 11-14 are connected directly to the four counter inputs, pins 16-19. In this way the three least significant digits are retained in the latch and the three most significant digits of the latch are set to the current temperature. The three least significant digits in the latch store the current rate of change of temperature which is calculated during subsequent periods of the program.

During P3, the MK 50395 counter is reset.

During P4, the MK 50395 counter is again ready to

THERMOMETER TIMING



count the pulses produced by the temperature-sensing oscillator for an entire period, during which the content of the register is ignored.

During P5, the sign flip-flop is reset so that the MK 50395 counter counts down during the following period. During P6, the MK 50395 is again ready to count up the temperature sensitive oscillator for one half cycle, and count down from the state arrived at at the end of P4. If the temperature has not changed in the interval between P4 and P6, the MK 50395 counter will stand at zero at the end of P6. If the temperature has decreased since P4, the counter will stand at some number which is proportional to the rate of change in temperature.

If the temperature has increased between P4 and P6, the MK 50395 counter is counted down to zero before the end of P6. When this occurs the sign flip-flop is set, and the level at pin 40 goes high, changing the mode of counting from down to up. At the end of P6, the MK 50395 counter stores a quantity which is proportional to the rate of change of temperature. If the sign flip-flop remains reset after P6, it provides a signal to the negative sign display associated with the rate display.

The durations of the periods of the negative-going half-cycle of the program oscillator are chosen so that the rate identifying contents of the MK 50395 counter are in units of degrees-per-hour. Since the change of temperature is less than 1000 per hour, only the lowest three digits of the counter contain significant information, with the three higher orders standing at zero. During P7, the current temperature data from the three highest digits of the latch are set into the counter by bringing the load counter pin 31 high from the leading edge of D1 thru D4. The contents of the counter are then stored in the latch by bringing pin 15 up after a delay. The program counter is reset to zero at P0 and the entire program is repeated successively. Display of temperature and rate of change is continuous, with the negative sign blanked during P5 and P6.

The temperature calibration data is entered into the register by operation of several manual switches. The CD4043 latches allow the digits of the BCD Register to be loaded individually and not alter the data in other digits.

Switches CD and RC are provided for disabling the program counter and for resetting the program counter (and the program oscillator.)

To load the BCD register, close the reset counter (CD) switch, select the desired BCD data with the register data switches, then depress the desired digit switch and the load data switch at the same time. After all digits have been properly loaded, check operation to assure the proper data has been loaded.

The period of the positive-going half-cycle of the program oscillator is chosen to allow calibration of the temperature. The period of the negative-going half-cycle of the program oscillator (P0, P2, P4, and P6) is chosen independently of the positive-going half-cycle to allow calibration of the rate of change.

Where the period of the positive-going half-cycle is P (in seconds), the period of the negative-going half-cycle is chosen equal to $\frac{p^2}{3.6 \cdot P}$ or the frequency of the program oscillator is chosen equal to $\frac{3.6 \cdot P}{3.6\ P}$ This allows calibration for both temperature and rate of change without any restriction on the temperature-sensitive oscillator.

The timing diagram above indicates the relative contents of the MK 50395 counter during the eight program periods.

MOSTEK®

SIX-DECADE COUNTER/DISPLAY DECODER

MK50398/9

FEATURES

☐ Single power supply

☐ Schmitt Trigger on the count-input

☐ Six decades of synchronous up/down counting

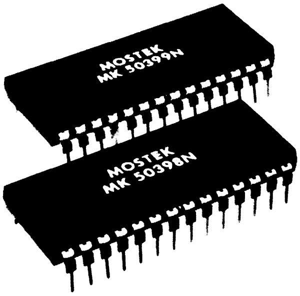
☐ Look-ahead carry or borrow

☐ Loadable counter

☐ Multiplexed 7-segment outputs, MK50398N

☐ Multiplexed BCD outputs, MK50399N

☐ Internal scan oscillator

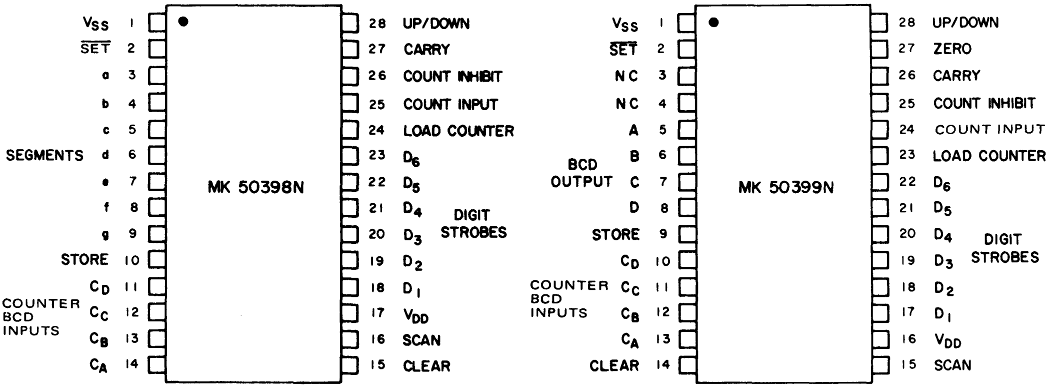


DESCRIPTION

The MK 50398/9 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with storage latches. The counter can be loaded digit-by-digit with BCD data and has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD or 7-segment format to the output. These devices are intended to interface directly with the standard CMOS logic families.

PIN CONNECTIONS FIGURE 1



OPERATIONS:

SIX-DECADE COUNTER, LATCH

The six-decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input. Count inhibit must remain high while the count input is high to inhibit counting.

The counter will increment when the up/down input is high (Vss) and will decrement when the up/down input is low. The up/down input can be changed 0.75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six-digit latch or the scan counter.

As long as the store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when the store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit-by-digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at Vss 2 micro-seconds prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

INPUTS, OUTPUTS

The seven segment outputs are open drain and capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at Vss. The Carry, Equal, Zero, BCD and digit strobe outputs are push-pull and are on when at Vss. All inputs except Counter BCD and the SCAN input are high-impedance CMOS compatible.

Two basic outputs originate from the counter: Zero output, and Carry output. Each output goes high on the positive- (Vss) going edge of the count input under the following conditions:

The Zero output goes high for one count period when all decades contain zero. During a load counter operation, the Zero output is inhibited. The Zero output is on the MK 50399 only.

The Carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999 when counting down and goes low with the negative going edge of the same count input. During a load counter operation, the Carry output is inhibited.

A count frequency of 1.5MHz can be achieved if the Zero output and Carry output are not used. These outputs do not respond at this frequency due to their output delay, as illustrated on the timing diagram, Figure 3.

BCD & SEVEN-SEGMENT OUTPUTS

Figure 3

BCD or seven-segment outputs are available. Digit strobes are decoded internally by a divide-by-six Johnson counter. This counter scans from MSD to LSD. By bringing the SET input low, this counter will be forced to the MSD decade count. During this time, the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when SET is low. Applying Vss to SET allows normal scan to resume. Digit 6 output is active (Vss) until the next scan clock pulse brings up the digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Typically, the interdigit blanking time is 3 to 10 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore, the BCD output data is valid when the positive transition of a digit output occurs. BCD outputs are on the MK 50399 only.

SCAN OSCILLATOR

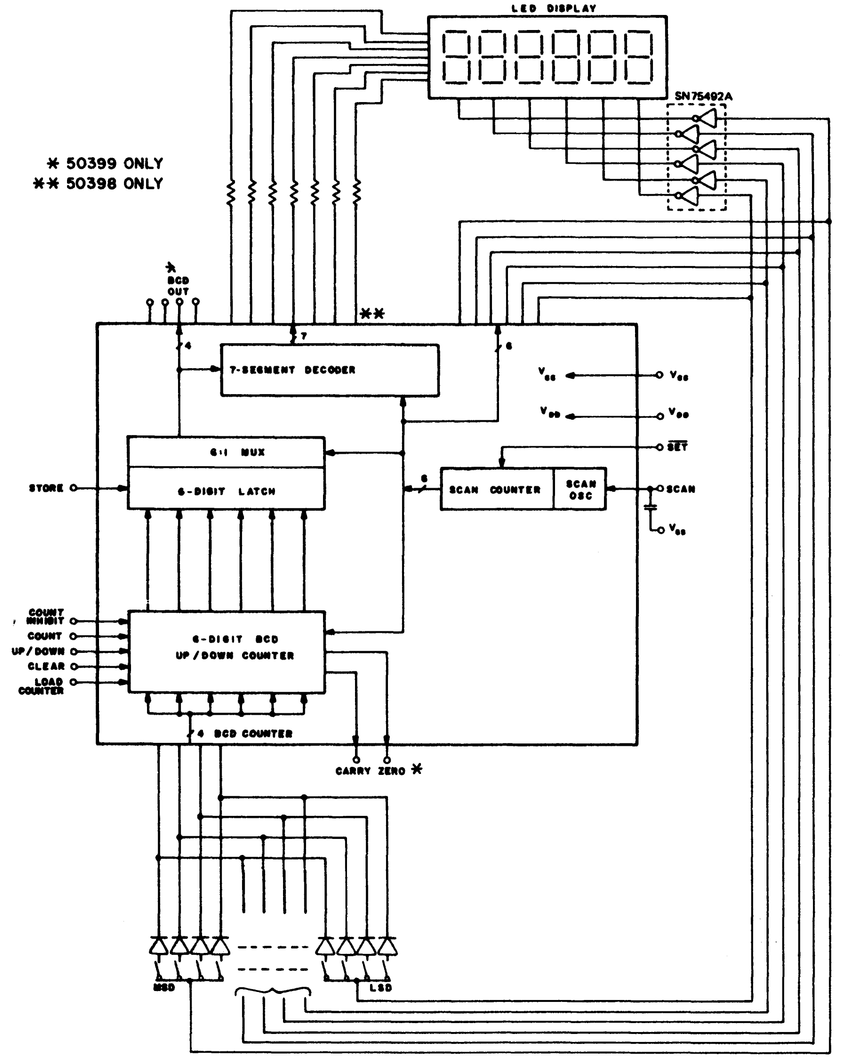
The counters have an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between Vss or VDD and the scan input. The wave form present on the scan oscillator input is triangular in the self-oscillate mode. An external oscillator may also be used to drive the scan input.

In the external drive mode, the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self-oscillate blanking time (3 → 10 μsec). Display brightness can be controlled by the duty cycle of the external scan oscillator.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from Vss to the Scan input:

	Min	Max
820pF	1.4kHz	4.8kHz
470pF	2.0kHz	6.8kHz
120pF	7.0kHz	20kHz

FUNCTIONAL DIAGRAM
FIGURE 2



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS}	+0.3V to −20V
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range (Ambient)	−40°C to +100°C

MAXIMUM OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply Voltage (V_{DD} = 0V)	10	15	V	
I_{SS}	Supply Current		40	mA	1
B_V	Break-Down Voltage (Segment only @ 10 μA)		V_{SS}−26	V	MK 50398 only
P_D	Power Dissipation		670	mW	2

ELECTRICAL CHARACTERISTICS

(V_{DD} = 0V, V_{SS} = + 10.0V to + 15.0V, 0°C $\leqslant T_A \leqslant$ 70°C)

STATIC OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Voltage, "0"	V_{DD}	20% of Vss	V	
V_{IH}	Input High Voltage "1"	V_{SS}−1	V_{SS}	V	3
V_{OL}	Output Voltage "0" @ 30 μA		20% of Vss	V	4
V_{OH}	Output Voltage "1" @ 1.5mA	80% of Vss		V	4
I_{OH}	Output Current "1"				
	Digit strobes	3.0		mA	5
	Segment outputs	10.0		mA	6
I_{SCAN}	Scan Input Pullup Current @ 0V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15V	2	40	μA	
I_{SET}	SET Input Pullup Current @ 0V	5	60	μA	

NOTES:

1. I_{SS} with inputs and outputs open at 0°C 28mA at 25°C and 25mA at 70°C. This does not include segment current. Total power per segment must be limited so as not to exceed power dissipation of package. (Θ_{JA} = 100°C/Watt)
2. All outputs loaded.
3. MIN V_{IH} from C_A C_B C_C C_D inputs is V_{SS} -3.5V. Those inputs have internal pulldown resistors to V_{DD}.
4. This applies to the push-pull CMOS compatible outputs. Does not include digit strobes or segment outputs.
5. For V_{OUT} = V_{SS} -2.0 volts. Average value over one digit cycle.
6. For V_{OUT} = V_{SS} -3.0 volts. Average value over one digit cycle.

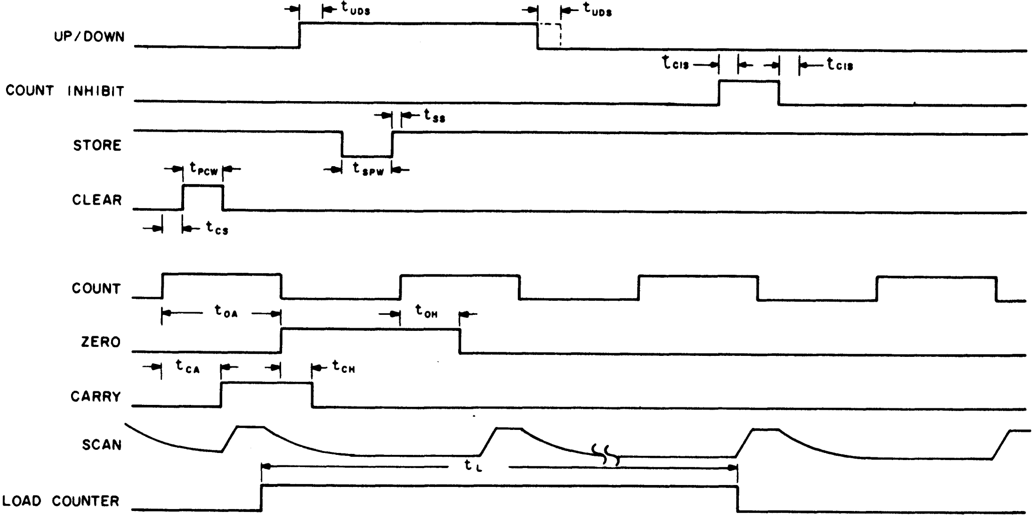
DYNAMIC OPERATING CONDITIONS

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.5	MHz	7,8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	325		ns	9
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Setup Time	0		μs	10
t_{CIS}	Count Inhibit Setup Time	0		μs	10
t_{UDS}	Up/Down Setup Time	- 0.75		μs	10
t_{CPW}	Clear Pulse Width	2.0		μs	10
t_{CS}	Clear Setup Time	–0.5		μs	10
t_{OA}	Zero Access Time		3.0	μs	10 50399 only
t_{OH}	Zero Hold Time		1.5	μs	10 50399 only
t_{CA}	Carry Access Time		1.5	μs	10
t_{CH}	Carry Hold Time		0.9	μs	11
t_L	Load Time	1/6 f_{SI}			12

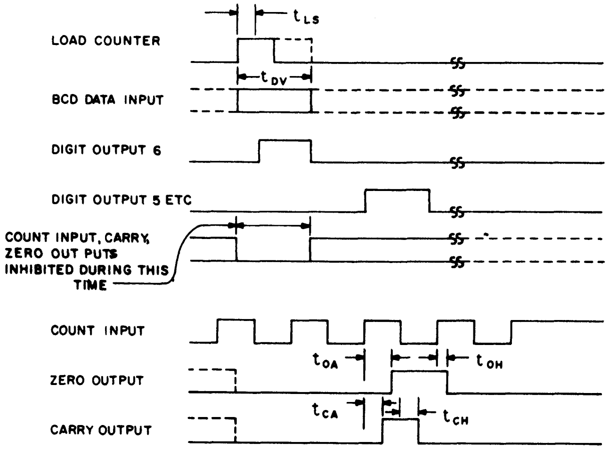
NOTES:

7. Measured at 50% duty cycle.
8. If Carry or Zero outputs are used, the count frequency will be limited by their respective output times.
9. The count pulse width must be greater than the carry access time when using the carry output.
10. The positive edge of the count input is the t = 0 reference.
11. Measured from negative edge of count input.
12. Time to load one digit.

TIMING
FIGURE 3



LOADING COUNTER, REGISTER (1 DIGIT)
FIGURE 4



t_{LS} 2.0 µsec min NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 µsec min NOTE: REF TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:

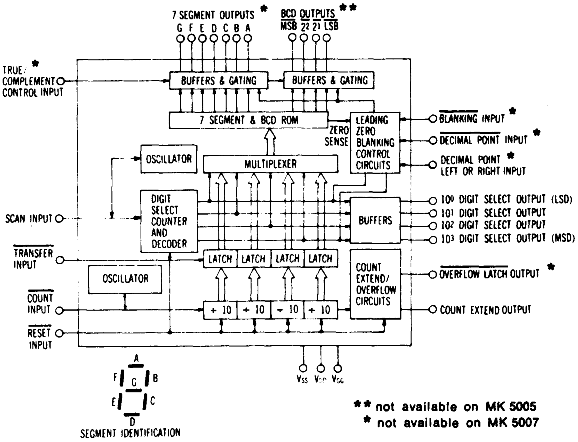
The inhibit function of the zero or carry output does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 µsec prior to a positive transition of a digit output.

MOSTEK®

4-DIGIT COUNTER / DISPLAY DECODER

MK5002/5/7

FUNCTIONAL DIAGRAM



** not available on MK 5005
* not available on MK 5007

GENERAL DESCRIPTION

The MK 5002/5/7 is an ion-implanted, P-channel MOS four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MK 5002/5/7 provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the Scan Input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low threshold voltages for input DTL/TTL compatibility are achieved through Mostek's ion-implanation process. Enhancement mode, as well as depletion-mode, devices are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25mW of power.

The functional diagram shows all options available on the MK 5002 MOS/LSI. Other members of this family which are different pin-outs of this same chip are the MK 5005 and MK 5007. The MK 5005 is supplied in a 24-pin package and does not include the BCD outputs. The MK 5007 is supplied in a 16-pin package. (See the pin diagrams for these members of the counter/display decoder family).

TRUTH TABLES

INPUT TRUTH TABLE

Input	Logic Condition to Activate
$\overline{\text{Count}}$	Negative Edge
$\overline{\text{Reset}}$	0
$\overline{\text{Transfer}}$	0
Scan	1 (Negative Edge increments Digit Select Counter)
True/Complement	1 = True Data 0 = Complementary Data
$\overline{\text{Decimal Point}}$	0
$\overline{\text{Blanking}}$	0
Decimal Point Left or Right	1 = Left 0 = Right

7-SEGMENT & BCD OUTPUTS
TRUTH TABLE

		DISPLAY SEGMENT							BCD			
Digit	Scan	a	b	c	d	e	f	g	$\overline{\text{MSB}}$	$\overline{2^2}$	$\overline{2^1}$	$\overline{\text{LSB}}$
0	1	0	0	0	0	0	0	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	0
2	1	0	0	1	0	0	1	0	1	1	0	1
3	1	0	0	0	0	1	1	0	1	1	0	0
4	1	1	0	0	1	1	0	0	1	0	1	1
5	1	0	1	0	0	1	0	0	1	0	1	0
6	1	0	1	0	0	0	0	0	1	0	0	1
7	1	0	0	0	1	1	1	1	1	0	0	0
8	1	0	0	0	0	0	0	0	0	1	1	1
9	1	0	0	0	0	1	0	0	0	1	1	0
x	0	1	1	1	1	1	1	1	1	1	1	1

True/Complement = Logic 1

TRUTH TABLE, OTHER OUTPUTS

Output	True Logic State	Time of Occurence
Digit Select Outputs	1	One-of-four, following Scan Input rising edge; all off when Scan Input is low.
$\overline{\text{Overflow}}$ Latch	0	Occurs on the 10,000th Count Input following a reset. Remains true until an external reset is accomplished.
Count Extend	1	Occurs each time the counter state attains 9,999 count. Remains true only until the next Count Input or Reset occurs (when the counter returns to 0,000).

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	MAX	TYP	UNITS	NOTES
T_A	Operating Temperature Range	0	75		°C	
V_{SS}	Supply Voltage	4.5	7.5		V	1,2
V_{GG}	Supply Voltage	V_{DD}	−13.2		V	1,2

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{GG} = V_{DD} = 0V; 0℃ $\leqslant T_A \leqslant$ 70℃ unless otherwise noted)

		PARAMETER	MIN	MAX	TYP	UNITS	NOTES
D.C. CHARACTERISTICS	V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}+0.8	V_{DD}	V	
	V_{IH}	Input Voltage, Logic 1 (High)	V_{SS}−1	V_{SS}+0.3	V_{SS}	V	3
	I_{SS}	Supply Current, V_{SS}		5.0	2.5	mA	4, Inputs open
	I_{GG}	Supply Current, V_{GG}		0.5	0.2	mA	V_{GG} = −12V
	C_{in}	Input Capacitance		10	3	pF	T_A = 25°C; f = 1MHz; V_{IN} = V_{SS}
	I_{IL}	Input Current, Logic 0, Count Input		1.6		mA	5
		Scan Input		1.6		mA	5
		Decimal Point Input		1.0		µA	
		Other Logic Inputs		1.0		mA	
	I_{OL}	Output Current, Logic 0	0.5			mA	6, V_{GG} = −12V
	I_{OH}	Output Current, Logic 1	0.5			mA	6, V_{GG} = −12V
	V_{OL}	Output Voltage, Logic 0		V_{DD}+0.2		V	4
	V_{OH}	Output Voltage, Logic 1	V_{SS}−0.2			V	4
DYNAMIC CHARACTERISTICS	f_{CI}	Count Input Frequency	DC	250		kHz	
	f_{SI}	Scan Input Frequency	DC	50		kHz	
	t_{RD}	Reset-to-Any Output Delay		15		µs	
	t_{PW}	Logic 0 Pulse Width, Reset Input	1.0			µs	
		Count Input	1.0			µs	
		Scan Input	10.0			µs	
		Transfer Input	2.5			µs	
	t_{PH}	Logic 1 Time Count Input	3.0			µs	
		Scan Input	10.0			µs	
	t_{SD}	Scan-to-Output Disable Time					
		Digit Select Outputs		15		µs	7
		All Data Outputs		15		µs	7
	t_{SE}	Scan-to-Output Enable Time					
		Digit Select Outputs		15		µs	8
		All Data Outputs		15		µs	8
	t_{CE}	Count Input-to-Count Extend Delay to 1 or 0		15		µs	9
	t_{OF}	Count Input-to-Overflow Delay (On)		15		µs	9
	t_{ROF}	Reset Input-to-Overflow Delay (Off)		5		µs	

NOTES:

1. V_{DD} = 0V
2. V_{SS}/V_{GG} differential no more than 25V.
3. Internal pull-up resistors (approx 10k Ohm) are provided at all inputs other than Count Input, Scan Input, and Decimal Point Input.
4. V_{GG} = −12V ± 10%. Outputs open.
5. Measurement made at V_I = V_{DD} + 0.4V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6 mA. 400 µA source current at V_{SS} −1.0 is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at V_O = V_{SS} −0.75V. (Direct driving base of PNP with emitter tied to +5).
   I_{OH} measured at V_O = V_{DD} + 0.75. (Direct driving base of NPN with emitter tied to V_{DD}).
7. Delay measured from the negative edge of the Scan Input.
8. Delay measured from the rising edge of the Scan Input.
9. Delay measured from the negative edge of the Count Input.

DESCRIPTION OF OPERATION

(Further information on the operation of Mostek's family of 4-digit Counter/Decoders may be found in the MK 5002 Application Report).

COUNTER LOGIC & TIMING

The Decade counters are synchronously incremented on the negative edge of the Count Input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

SCAN CONTROL LOGIC & TIMING

The Digit-Select Counter is incremented by a negative edge on the Scan Input. During the time the Scan Input is at 0, the 7-segment and Digit-Select outputs are forced off and the complement BCD outputs are forced to logic 1. The off level of the 7-segment and BCD outputs is determined by the state of the True/Complement input. (See Truth Tables.) This remains until the Scan Input returns to logic 1.

The Digit-Select Counter is a one-of-four counter, scanning from MSD (Most Significant Digit) to LSD (Least Significant Digit), enabling one quad latch output at a time, and presenting a logic 1 to the corresponding Digit-Select output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

TRANSFER LOGIC & TIMING

While the Transfer input is a logic 0, data in the decade counters is transferred to the static storage latches. This input may be left at 0 for a continuous transfer-and-display mode, or may be pulsed periodically to store only on command.

Termination of a transfer command occurs internally when the input is taken to a logic 1 and the next Count Input negative edge occurs. This allows asynchronous Count and Transfer operation since the transfer is terminated prior to incrementing the counters. This means that a Count Input negative edge must follow a Transfer command before a Reset is applied to prevent transfer of invalid data. An external Reset Command must be delayed at least one Count Input negative edge following a Transfer. External transfer should terminate at least 1 μs prior to this Count negative edge and Reset should occur no sooner than 1 μs following that edge.

RESET CONTROL

The decade counters are reset to 0,000 when the Reset Input is at logic 0. The Reset Input at logic 0 also forces the Scan to the MSD output and resets the Overflow Latch output to a logic 1 (if previously latched to a logic 0). It maintains this condition as long as the logic 0 is present at the Reset Input and overrides all other associated inputs. As indicated previously, the decade counters should not be reset until a transfer has been terminated.

Since the Reset Input resets the Scan Counter to MSD, the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, FScan must be much greater than four times FReset.

Ideally, the Reset pulse should also be made narrow to prevent its duration from causing the MSD to be ON much longer than the other digits and thus appear to be brighter.

LEADING ZERO BLANKING

At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or the Decimal Point Input is clocked. Any number following will be displayed. Leading zero blanking does not affect the BCD outputs or the LSD in the display which is displayed even if zero. The LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.

The Decimal Point Input pin should be brought to logic 0 at the time the character is enabled that contains the decimal point. The first non-zero number or the Decimal Point Input signal in the scan cycle puts the blanking circuitry in the unblanking mode. If the Reset In (forces the Scan Counter to the MSD) occurs when the circuit is in the unblanked mode, the first complete MSD to LSD scan will be done in the unblanked mode. This could result in a dimly displayed leading zero. A simple solution to this problem would be to force the Blanking Input low during a reset and release it only after an LSD has occurred.

Leading zero blanking may be inhibited by wiring the Decimal Point Input to ground. The MK 5007 does not have a pin for Decimal Point Input and therefore does not have leading zero blanking.

OTHER INPUTS

The Blanking Input at logic 0 forces the 7-segment outputs to the off-state and the BCD to the equivalent of the number zero. This condition is maintained on a DC basis as long as the Blanking Input is 0. The Digit-Select outputs continue to operate at the scan rate as described.

A True/Complement control inverts both BCD and 7-segment outputs when at logic 0. Depending upon the display used, combinations of the Blanking Input and True/Complement Control can be chosen to give a lamp test.

The Decimal Point Left or Right control allows the use of displays with the decimal point physically located on the left or right of the numeral. Logic 1 is decimal-point-left. In the right mode, even though the $\overline{\text{Decimal Point Input}}$ is clocked, unblanking is delayed until the following digit is enabled.

OUTPUTS

All output buffers on the MK 5002 family are push-pull. A negative power supply terminal, V_{GG}, is provided to increase the drive capabilities of these output buffers. Since the V_{GG} supply is connected only to these output buffers, it has no effect on any other device characteristics.

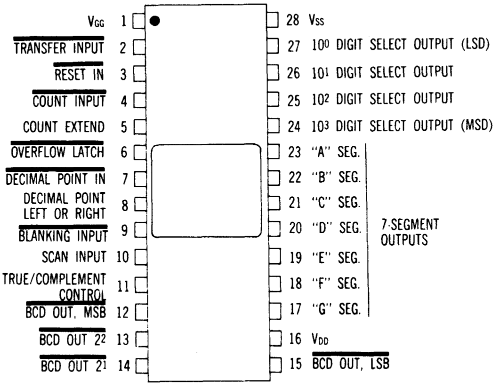
Output characteristics are covered in the MK 5002 Application Report which illustrates the effects of V_{GG} with current to be expected at various output voltages.

The outputs are designed to drive directly to the base of common-emitter transistors, so that output voltage is clamped or maintained at a potential where the MK 5002 is able to sink or source its greater amount of current.

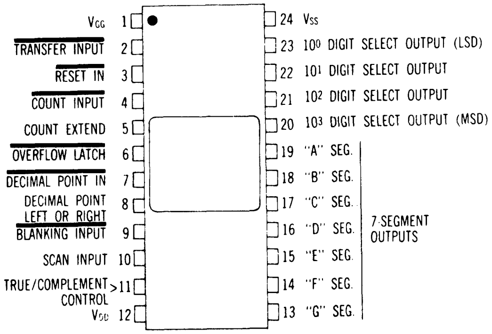
PIN CONNECTIONS

The MK 5002/5/7 is available in a 28-pin dual in-line package, a 24-pin dual in-line package, and a 16-pin dual in-line package. Only the 28-pin package contains all available functions.

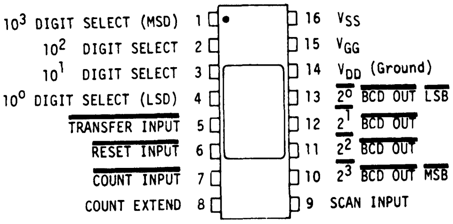
MK 5002P
MK 5002N



MK 5005P
MK 5005N



MK 5007P
MK 5007N



MOSTEK®

MK5002/7

Application Note

USING THE MK5002/ MK5007 MOS 4-DIGIT COUNTER CIRCUITS

Using The MK 5002/MK 5007 MOS 4 Digit Counter Circuits

INTRODUCTION

This Applications Note describes the functional features of Mostek's MK 5002 and MK 5007 low-power counter circuits. Interfacing to LED, incandescent, and gas-discharge displays is described. Cascading of circuits to provide a display of eight or more digits, and an annunciator application are also included.

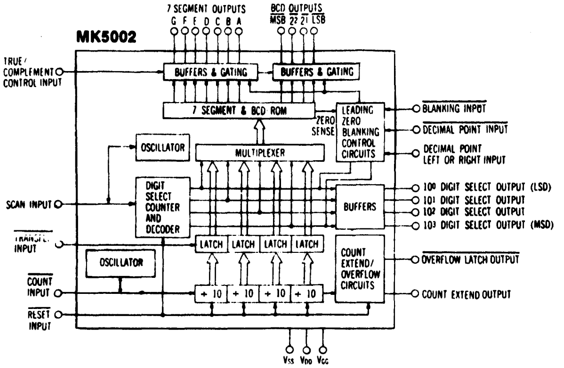
The MK 5002 P is an MOS counter circuit containing internal synchronous, 4-decade counters, static storage latches, BCD and 7-segment outputs, multiplex logic and leading-zero blanking circuitry. The MK 5007 P is identical to the MK 5002 P, except that the 7-segment outputs, leading-zero blanking controls, and other connections have been omitted in order to provide a counter circuit in a 16-pin package. Complete functional descriptions and specifications for the MK 5002 and MK 5007 are included in the data sheet for these products.

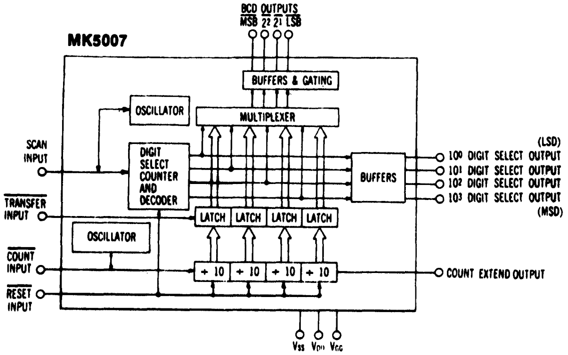
DESCRIPTION OF OPERATION

Negative-edge transitions at the Count Input increment the ÷ 10,000 counter. This counter's state is set in the latches when the Transfer Input is low (logic 0). The Scan Input drives an internal ÷ 4 counter, routing one decade count at a time to the output via the 7-segment decoder. The selected digit is indicated via the Digit Select output.

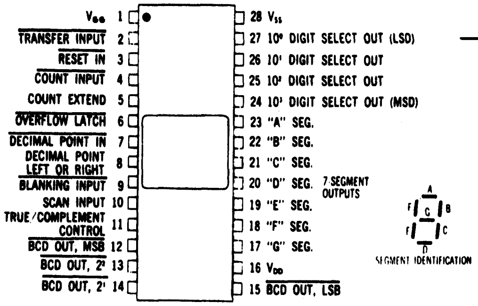
The decoders are scanned from MSD (Most Significant Digit) to LSD (Least Significant Digit). Leading zeros, i.e., zeros which precede the non-zero numbers or the decimal point, are automatically blanked on each MSD to LSD scan, with the exception of the LSD, if selected with the MK 5002. Leading zero blanking is not available with the MK 5007.

FUNCTIONAL DIAGRAM

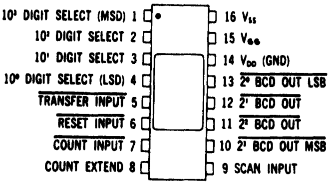




MK5002P
PIN CONNECTIONS



MK5007P
PIN CONNECTIONS



STROBED OPERATION

When strobing LED's (Light-Emitting Diodes), only one character in the display is illuminated at any one time. However, a sufficiently fast strobe rate will allow the human eye to integrate the display, resulting in apparently flicker-free characters.

Since LED's are diodes and therefore inherently unidirectional, the MK 5002 seven-segment lines may be common to all four LED 7-segment inputs. The Digit Select outputs provide the necessary control to ensure that only one character is enabled at any one time. As a result, only one buffer/driver is required per 7-segment line. This buffer need only be capable of handling the current for a single segment since it is never required to drive more than one segment at a time. The Digit Select buffer/driver, however, controls one entire character and therefore must handle the current required by up to seven separate segments plus the decimal point, if used.

The apparent brightness of the display is approximately proportional to the average current. To produce a given brilliance in a 4-digit display equal to the brilliance in a single, continuously-ON, digit would require four times the peak current required for the single digit. For example, if, for a single digit, maximum (peak) current, I_{FRM}, equals average current, $I_{F(AV)}$, at 5 mA per segment, then in a 4-digit display I_{FRM} of 20 mA per segment will be required to produce $I_{F(AV)}$ of 5 mA resulting in equal brilliance.

OPERATING CONSIDERATIONS

Operating Considerations and Restrictions

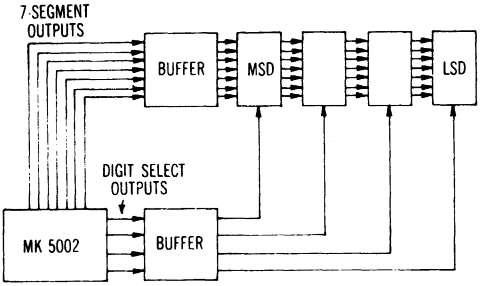
The external Reset Input forces the scan control logic to MSD (Most Significant Digit). This condition will be maintained as long as the Reset is applied (Reset at logic O, low state). The reset duration can then cause a variation in brilliance of the MSD (as compared to the other digits). This effect should be considered in determining system timing.

It should also be noted that if the periodic reset is applied at a rate faster than the scan rate, the less significant digits will never be allowed to turn on. Therefore, F_{Scan} must be much greater than four times F_{Reset}. Ideal timing would combine narrow reset pulses with the frequency of reset pulses low compared to the frequency of the scan pulses.

Transfer Operations

Transfer of any counter state begins with the Transfer Input low but does not terminate until after the Transfer Input is taken back high *and* the next Count Input negative edge occurs. This feature allows the Count Input and Transfer to be operated asychronously but restricts the use of a reset pulse following a transfer pulse. ***To prevent the possible transfer of invalid data, an external Reset Command must be delayed at least one Count Input pulse (negative transition) following a transfer.***

FIG. 1: 4-DIGIT LED DISPLAY SYSTEM



OUTPUT CHARACTERISTICS

The MK 5002/7 outputs were designed to drive common-emitter transistors. Output sink current is specified with the output directly driving the base of a PNP transistor whose emitter is connected to the V_{SS} potential. Output source current is specified with the output directly driving the base of an NPN transistor whose emitter is connected to V_{DD} or ground. Therefore, in both cases the voltage at the output is clamped by the turned-on transistor. The MK 5002 provides a True/Complement input to select the desired logic state for a segment ON condition.

The curve shown in Fig. 2 reflects the guaranteed minimum sink/source available at the outputs at various potentials of V_{GG} (see Power Supply Considerations) with the following conditions:

1. Sink current measured at $V_O = V_{SS} - 0.75$ V (transistor clamp)
2. Source current measured at $V_O = V_{DD} + 0.75$ V (transistor clamp)
3. V_{DD} = ground
4. T_A = 75°C (worst-case for measurement)

FIG. 2: OUTPUT CURRENT vs SUPPLY VOLTAGE, V_{GG}
(at T_A = 25 C and T_A = 75 C)

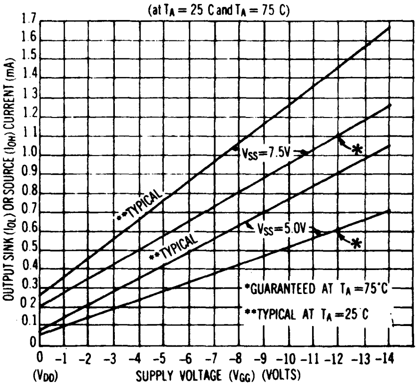


FIG. 3: TYPICAL OUTPUT CHARACTERISTICS
(at T_A = 75 C, V_{SS} =7.5V; V_{GG} =V_{DD} =0V)

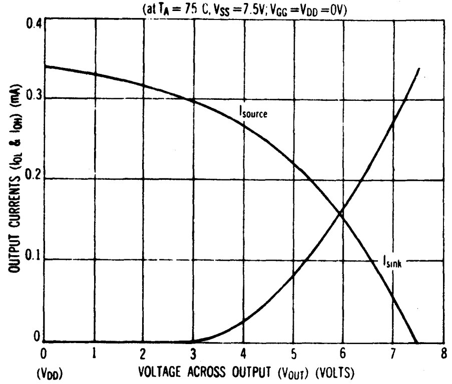


FIG. 4: TYPICAL OUTPUT CHARACTERISTICS
(at T_A = 75 C, V_{SS} = +5V, V_{GG} = V_{DD} -0 V)

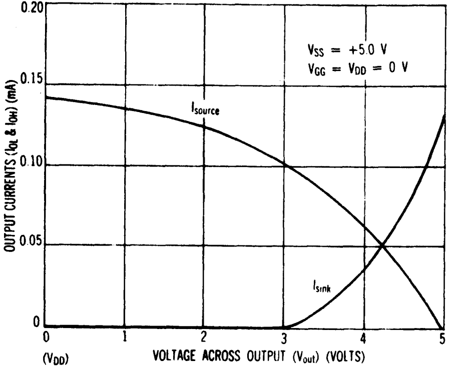
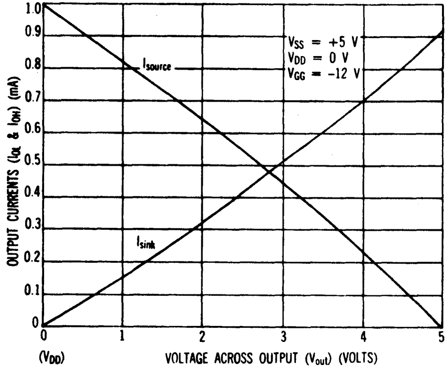


FIG. 5: TYPICAL OUTPUT CHARACTERISTICS
(at T_A = 75˚C, V_{SS} = +5V, V_{DD} = 0V; V_{GG} = -12V)



INTERFACING WITH LED'S AND OTHER NUMERIC DISPLAYS

NOTES:

(1) R_L is the current-limiting resistor and should be approximately:

$$R_L \times 10^3 = \frac{V_{SS} - V_{sat} - V_F}{4\ [I_{F(AV)}]}$$

V_{sat} = total for both transistors in segment lines and select lines

V_F = LED diode forward voltage drop

$I_{F(AV)}$ = diode current (in milliamperes)

(2) See Power Supply Considerations

FIG. 6: INTERFACING WITH COMMON-ANODE LED's
(SUCH AS MONSANTO MAN-1, TEXAS INSTRUMENTS TIXL 302, OPCOA SLA-1)

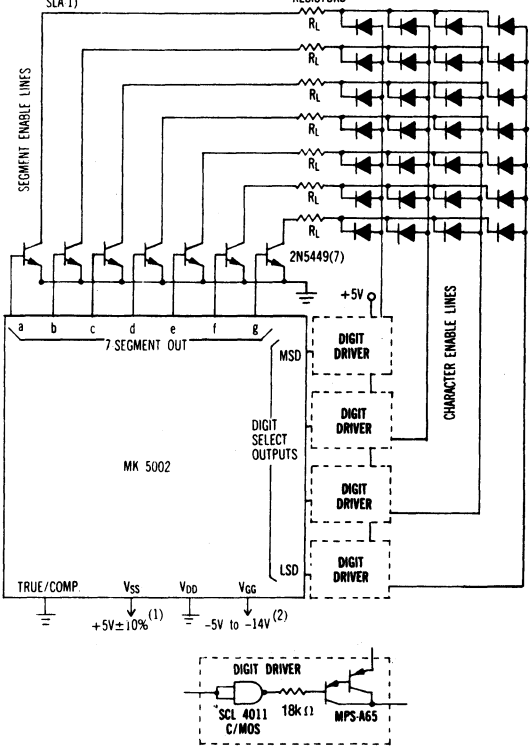


FIG. 7: INTERFACING WITH COMMON CATHODE LED's
(SUCH AS HEWLETT-PACKARD 5082-7200 SERIES, MONSANTO MAN-3)

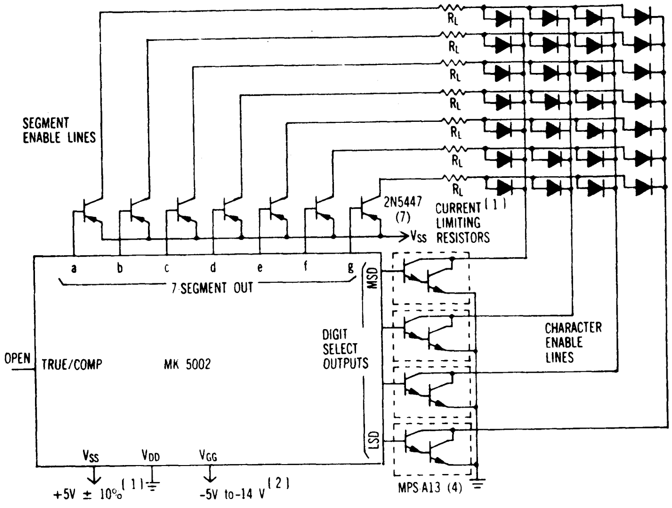


FIG. 8: INTERFACING WITH GAS DISCHARGE DISPLAYS
(SUCH AS SPERRY AND PANAPLEX II)

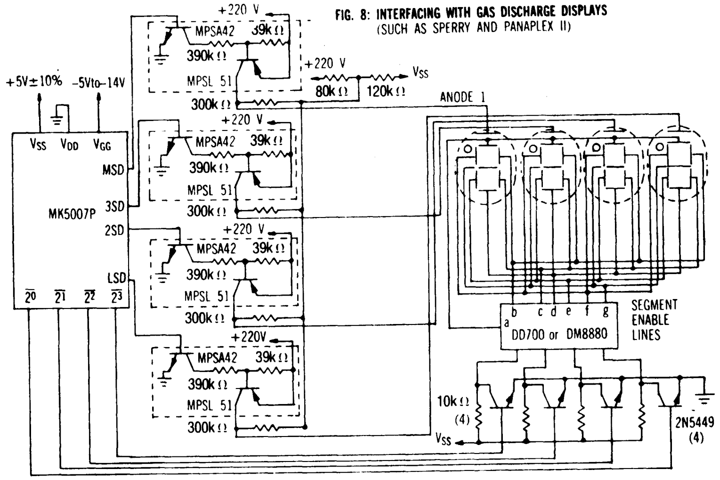
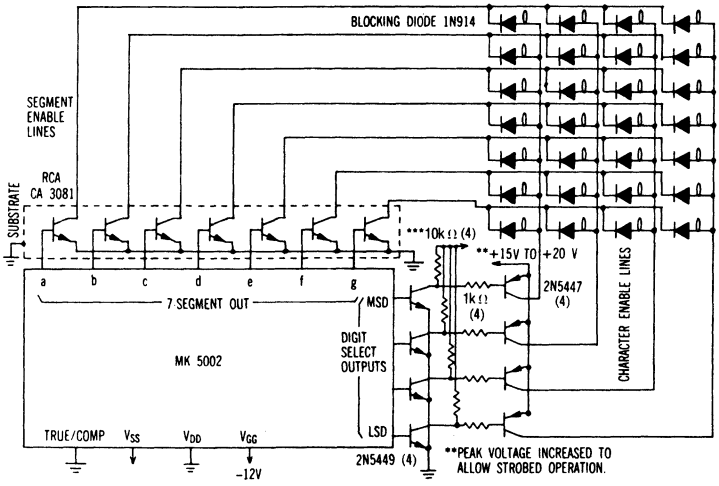


FIG. 9: INTERFACING WITH FILAMENT DISPLAYS
(SUCH AS SHELLY 3015 CN, PINLITE 03-15, LUMINETICS SERIES 90)



**PEAK VOLTAGE INCREASED TO ALLOW STROBED OPERATION.

***ADDITIONAL RESISTOR ENSURES TOTAL SHUT-OFF OF PNP TRANSISTOR

POWER SUPPLY

Power Supply Considerations

All internal circuitry, including oscillators, of the MK 5002 operates from a single power supply, using only V_{SS} and V_{DD}. A provision is made, however, to bring in a more negative supply, V_{GG}, to increase the drive capability of the output buffers.

For applications where a single supply is desired the lack of drive in the output buffers must be compensated. In order to assure a rapid pull-down at the circuit outputs it is recommended that 100KΩ resistors be connected between the outputs and ground. In addition several things can be done to compensate for the lack of drive that the displays will experience. These include:

1. Increasing V_{SS}. See output sink-source characteristics in Fig. 2 and Fig. 3.
2. Selecting high-gain transistor buffers. (Refer to TI TIS 92 [NPN] and TIS 93 [PNP] transistors.)
3. Decreasing R_L value and increasing Scan Input duty cycle to be on (high state) more than 80% of the time.
4. Selecting red filter for GaAsP LED's to reduce background illumination and increase contrast.

See also Operating Considerations.

DECIMAL POINT CONTROLS

Decimal Point Control Blanking

As described previously, zeros preceding the decimal point are blanked (on the MK 5002 only). The negative edge of the Decimal Point Input sets the blanking circuit to the unblank condition. Therefore an input is required for each MSD to LSD scan cycle since the blanking circuit is reset to the blanking condition at each MSD occurrence. A convenient method of providing this clock input at the selected position is to use the Digit Select character enable lines, as illustrated in the following circuits. Since the Digit Select is a high-going signal when true, this signal must be inverted prior to entry to the Decimal Point Input (which requires a negative-going signal).

Decimal Point Left or Right

This feature is provided on the MK 5002 so that the device will operate displays with the decimal point physically located on the left or right of the selected digit. In the Decimal Point Right mode (Decimal Point control tied to ground), even though the Decimal Point input is triggered, unblanking will not commence until the next digit is enabled.

FIG. 10: CLOCKING DECIMAL POINT INPUT FOR COMMON-ANODE LED's

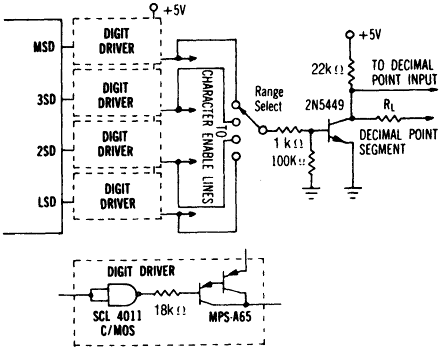
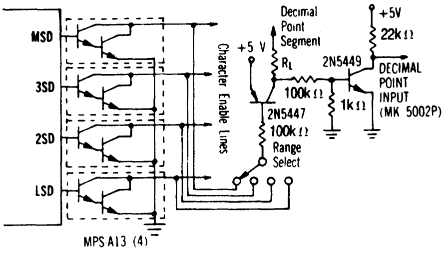


FIG. 11: CLOCKING DECIMAL POINT INPUT FOR COMMON-CATHODE LED's



INTERNAL OSCILLATORS

Count Oscillator

An internal Count Oscillator is provided for use where a constant input rate is desired (or it may be overridden by operating the Count Input directly from TTL/DTL levels). This feature provides a fixed time base for a count of 0 to 10,000, for use in such applications as DVM's (Digital Volt Meters) and A-D converters. A single capacitor on the input as shown in Fig. 12 may be used to control the oscillator frequency.

A resistor, shown as R_1, is not required, but may be used when desired to trim the frequency to a more exact setting. Typically, R_1 should be in the range of 30 k Ohms to 150 k Ohms. A value below about 30 k Ohms may prevent oscillation while resistances above 150 k Ohms have little effect.

Scan Oscillator

An internal Scan Oscillator is provided for use where a constant scanning or multiplexing rate is desired (or it may be overridden by operating the Scan Input directly from TTL/DTL levels). This feature provides an asynchronous scan rate requiring only a timing capacitor, as shown in Fig. 14, eliminating extra clocking circuits.

A trimming resistor may also be used, similar to that shown in Fig. 12, if desired. A trimpot tied to ground, shown here as R_2, may be used instead to control the duty cycle of the Scan Input. The lower the value of R_2, the less time the Scan Input is at high and the selected digit is ON. (Note that R_1 or R_2 may be used but not both.)

Without resistors, the duty cycle of any given digit is about twenty-four per cent.

FIG. 12: CAPACITOR ON COUNT INPUT

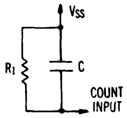


FIG. 13: TYPICAL COUNT INPUT OSCILLATOR FREQUENCY vs. CAPACITANCE
(At T_A = 25 C and V_{SS} = +5V)

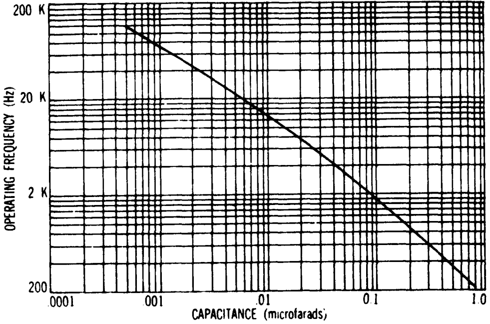


FIG. 14: CAPACITOR ON SCAN INPUT

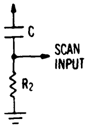


FIG. 15: TYPICAL SCAN INPUT OSCILLATOR FREQUENCY vs. CAPACITANCE
(at T_A=25 C and V_{SS}=+5V)

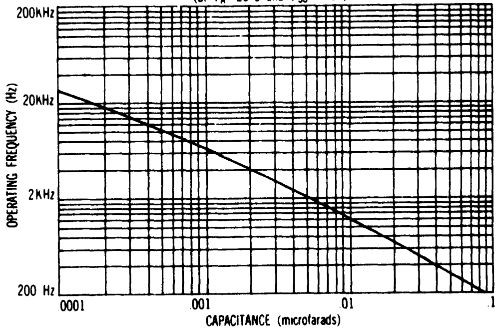
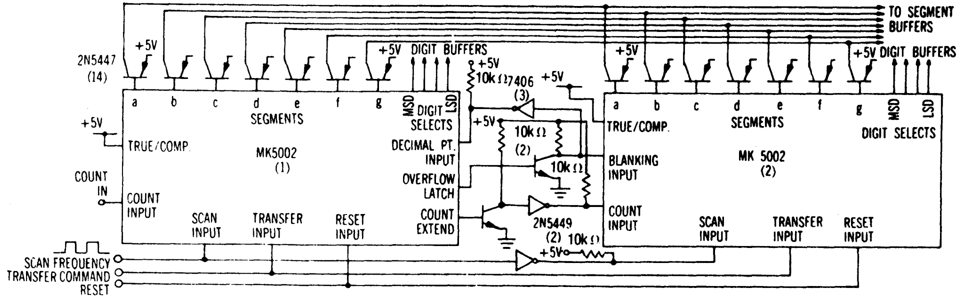


FIGURE 16: CASCADING TWO MK 5002



CASCADING THE MK 5002

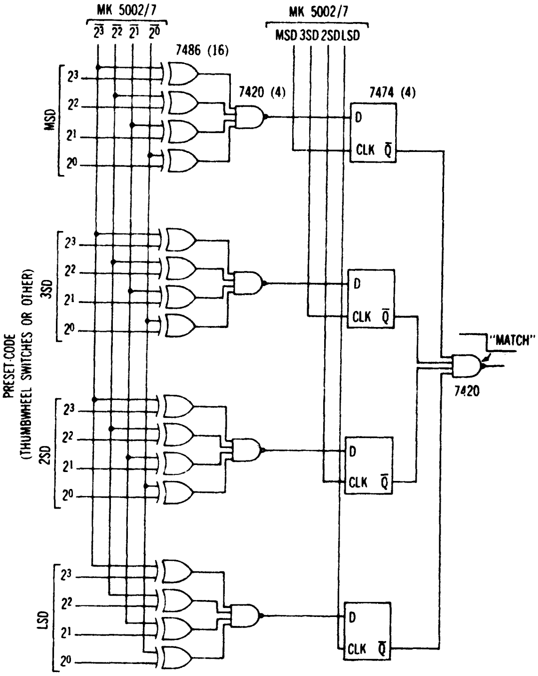
Two or more MK 5002 circuits can be conveniently cascaded when a display of more than four digits is required. Fig. 16 illustrates cascading with two MK 5002 circuits for an 8-digit display. Each segment output from the two circuits is buffered with a single-ended transistor buffer. This allows both circuits to be wired-ORed to the one set of seven segment lines from the 8-digit display. Each of the digit select outputs should be buffered to drive the corresponding display digit. Complement Scan Inputs are applied to the circuits. When the Scan Input is low on one device, the 7-segment outputs are high, the Digit Select outputs are low, and the corresponding display is unaffected by that device. The other device meanwhile displays one of its digits because its Scan Input is high. By making the Scan Input a square wave of greater than 500 Hz in frequency, each digit will be displayed an equal length of time. Additional logic is shown between the two 5002 circuits to retain leading zero blanking for the full eight digits. Until circuit (1) reaches a count of 10,000, circuit (2) has its blanking input held low, forcing all its segment lines high and preventing the least significant digit (zero) from being displayed by this circuit. After circuit (1) reaches a count of 10,000, its overflow latch output raises the blanking input on (2) and maintains this state until a reset condition occurs. The overflow latch output on (1) also forces the decimal input on (1) low so that leading zeros on this display will not be blanked. Without this provision the number 10,000 would be displayed as BBB1 BBBO resulting in a readout of 1 _ _ _0, [circuits (2) and (1), respectively, B = Blank]. With this feedback the correct number is displayed, BBB1 0000, or a readout of _ _ _1 0000.

USING THE MK 5002/5007 P IN ANNUNCIATORS/CONTROLLERS

In some applications where the MK 5002/7 is used as a totalizer or event counter it is desirable to select a predetermined count to halt or start an operation, or to set off an alarm. Fig. 17 shows one method of comparing the count of the MK 5002/7 with a preset BCD code. This code could be hard-wired or supplied by a BCD-encoded switch.

It should be noted that the digit strobes and complementary BCD data supplied by the MK 5002/7 will have to be buffered to drive the TTL loads. The frequency should also be greater than or equal to four times the Count frequency. This will prevent the count in the MK 5002/7 from changing before a complete cycle of all four digits can be made.

FIG. 17: USING THE MK 5002/7 WITH THUMBWHEEL PRESETS FOR CONTROL FUNCTIONS OR ANNUNCIATORS.



1980 INDUSTRIAL PRODUCTS DATA BOOK

I TABLE OF CONTENTS
II GENERAL INFORMATION
III FREQUENCY GENERATOR
IV DIGITAL ALARM CLOCK
V COUNTER DISPLAY DECODERS
VI COUNTER TIME BASE CIRCUIT
VII A/D CONVERTER ANALOG MULTIPLEXER

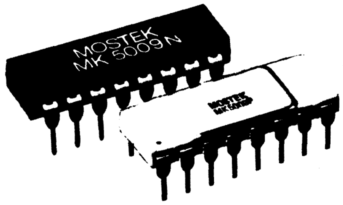
MOSTEK

COUNTER TIME-BASE CIRCUIT

MK5009

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- ☐ Operates DC to above 2MHz
- ☐ Binary-encoded for frequency selection



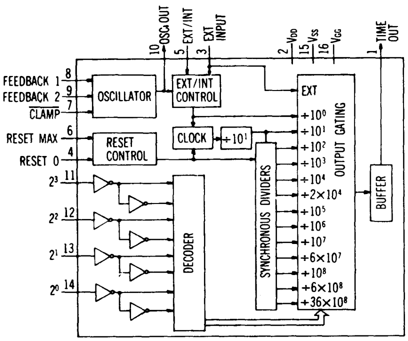
DESCRIPTION

The MK 5009 is a highly-versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load ion-implantation process and P-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 provides the basic time periods necessary for most frequency-measuring instruments, i.e., 1 µs through 100 seconds. One minute, ten-minute, and one-hour periods are also available using a 1MHz input. Using a 1/1.2MHz input, the MK 5009 can also provide a 50/60Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



TIME OUT

ADDRESS INPUTS				WITHOUT RESET	RESET		BYPASS MODES (see page 3)		
					Reset Max.	Reset Min.	Mode 1	Mode 2	Mode 3
2^3	2^2	2^1	2^0	$R_{MAX} = 0$ $R_O = 0$	$R_{MAX} = 1$ $R_O = 0$	$R_{MAX} = 0$ $R_O = 1$	$R_{MAX} = V_{GG}$ $R_O = 0$	$R_{MAX} = 0$ $R_O = V_{GG}$	$R_{MAX} = V_{GG}$ $R_O = V_{GG}$
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$	Resets counters to their highest states	Resets counters to their lowest states	$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$			$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$			$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$			$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$			$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6 \times 10^7$			$\div 6 \times 10^4$	$\div 6 \times 10^4$	$\div 6 \times 10^1$
1	0	1	0	$\div 36 \times 10^8$			$\div 36 \times 10^5$	$\div 36 \times 10^5$	$\div 36 \times 10^2$
1	0	1	1	$\div 6 \times 10^8$			$\div 6 \times 10^5$	$\div 6 \times 10^5$	$\div 6 \times 10^2$
	*			—			—	—	—
1	1	1	0	$\div 2 \times 10^4$			$\div 2 \times 10^1$	$\div 2 \times 10^1$	$\div 2 \times 10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset 0 inputs.

Logic 1 = High = V_{SS}

Logic 0 = Low = V_{DD}

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . + 0.3V to – 20V
Operating Temperature Range (Ambient) . . . . 0°C to + 70°C
Storage Temperature Range (Ambient) . . . . – 55°C to + 150°C

RECOMMENDED OPERATING CONDITIONS
($0°C \leqslant T_A \leqslant 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+ 4.5		+ 5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	– 9.6		– 14.4	V	
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	DC		200	kHz	
f_{EXT}	External Frequency	DC		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{\text{CLAMP}}$	—				Note 5
	Ext. Input	200			nsec	
t_{PH}	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			μsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG} + 1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS} + 0.3	V	

ELECTRICAL CHARACTERISTICS
(V_{SS} = +5V ± 10%; V_{DD} = 0V; V_{GG} = –12.0V ±20%; $0°C \leqslant T_A \leqslant 70°C$)

	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
I_{IL}	Input Current, Logic 0			– 1.6	mA	Note 2: V_I = 0.4V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL} = 1.6mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH} = – 40 μA*
f_{STA}	Frequency Stability w/ Volt. Change, RC Mode		± 3.0		%/V	Note 3
	/ Temp. Change, RC Mode		– 0.2		%/°C	
	Crystal Mode		—			Note 4
$t_{e\ e}$	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Supply Voltage Constant

† Typical values at V_{SS} = + 5V, V_{DD} = 0V, V_{GG} = – 12V, and T_A = 25°C
1. Logic inputs at V_{SS}, output-open circuited. Each logic input (see Note 2) contributes an additional 1.6mA (max) to I_{SS} when at logic 0.
2. Logic inputs are: Reset Max; Reset 0; Address inputs; Ext. Input; Ext/Int Select; and $\overline{\text{Clamp}}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at $\overline{\text{Clamp}}$ input is 50% of oscillator period.

*V_{OH}, V_{OL} apply only to Time Out.

DESCRIPTION OF OPERATION

The MK 5009 consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36×10^8 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8/RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When $\overline{\text{Clamp}}$ goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the $\overline{\text{Clamp}}$ (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. It operates in the parallel resonant mode. The crystal used should operate properly with a 5mW drive level and should have a loading capacitance (C_L) of 32pF. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = ½ C_L.

RESET/BYPASS CONTROL

The MK 5009 provides two different reset conditions. A positive-going pulse of 10 µs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009, that signal should be applied at the External Input (Pin 3), and the External/Internal Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

EXT/INT tied to V_{DD}

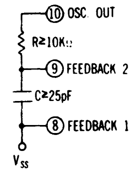


Figure 1

EXT/INT tied to V_{DD}

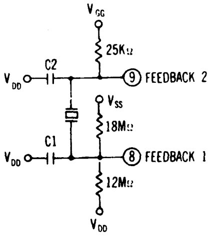
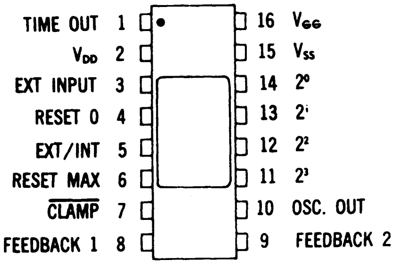


Figure 2

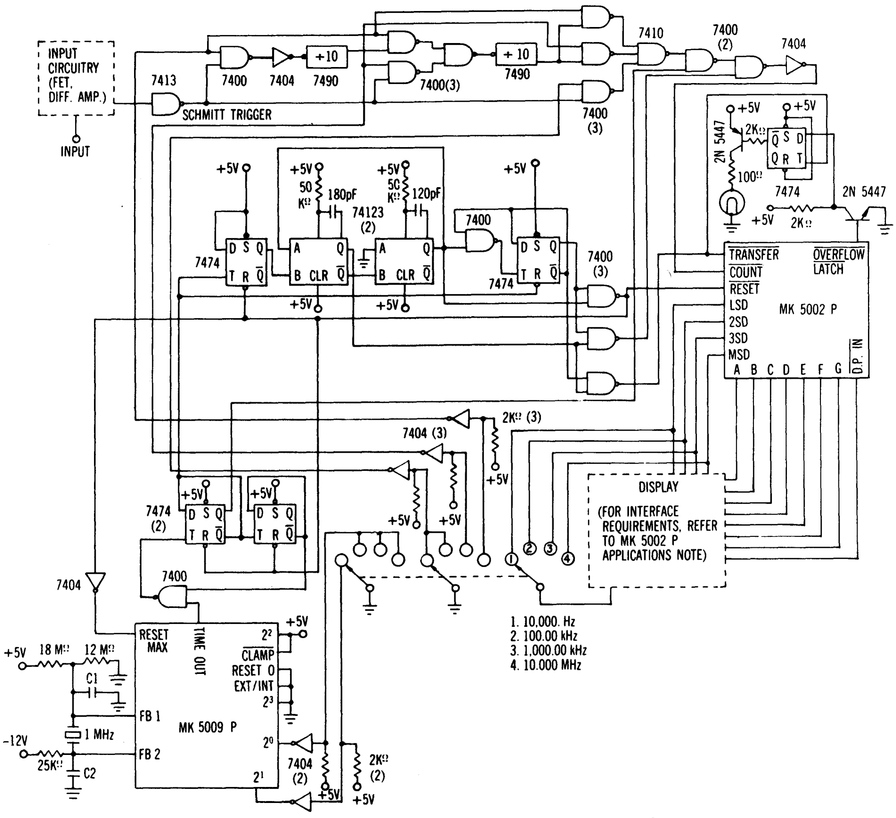
PIN CONNECTIONS



APPLICATION—10MHz Frequency Counter

The circuit shown below is a frequency counter capable of counting input rates up to 10MHz, selected in four ranges. The MK 5009 provides the time base intervals while the Mostek MK 5002 counter circuit provides counting, storage, and display functions. Two decades of prescaling using TTL are employed. TTL one-shots provide proper timing for the 5002.

To replace the functions of the MK 5009, an active device and Schmitt trigger for the crystal oscillator would be needed, plus six 7490's to achieve the correct time out. Replacing the functions of the MK 5002 would require four 7490's, and four BCD-to-seven-segment decoders.



MOSTEK

MK5009 COUNTER

Application Note

USING MOSTEK'S MK 5009 COUNTER TIME-BASE CIRCUIT

Using Mostek's MK 5009 Counter Time-Base Circuit

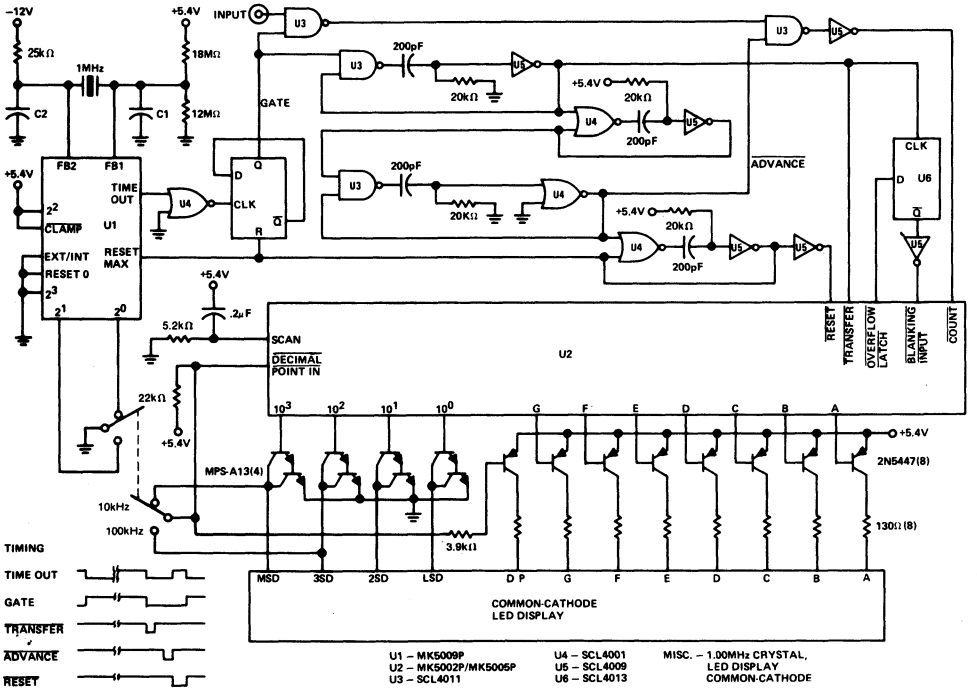
DIGITAL FREQUENCY METER

The 100 kHz frequency meter which can be battery operated is illustrated schematically in Figure 1. The +5.4V power required is supplied by four C cells and a series diode. Since most of the 200 mA required is used in the LED display, it is advantageous to employ a "push-to-read" function on the meter. This is easily accomplished by using either a MOSTEK MK 5002 or MK 5005 as the counting device and display driver. If an unconditional reset is applied to the U-6 flip-flop, to be released only when the display is to be read, the display normally will be blanked.

The circuit's input responds to a +5V signal. A more general purpose front end, if desired, could be added to the NAND gate U3. The range of the meter could also be expanded by using decade prescalers at the input.

The timing diagram in Figure 1 also shows the interface timing between the MK 5009 and MK 5002. Basic C/MOS one-shots are used to conserve power; but if battery operation is not required, standard TTL one-shots can be used. The four one-shots generate the following times; transfer pulse width (at the end of a measurement period); time delay between the transfer pulse and count negative edge; count negative edge; and reset pulse width. To obtain an accurate time-out interval on the MK 5009, a flip-flop is used to count two consecutive negative edges of the Time-Out output.

This simple circuitry gives a 4-digit frequency meter with crystal-controlled accuracy, typically requiring 8 mA from the positive supply and 5 mA from the negative supply, excluding display power.

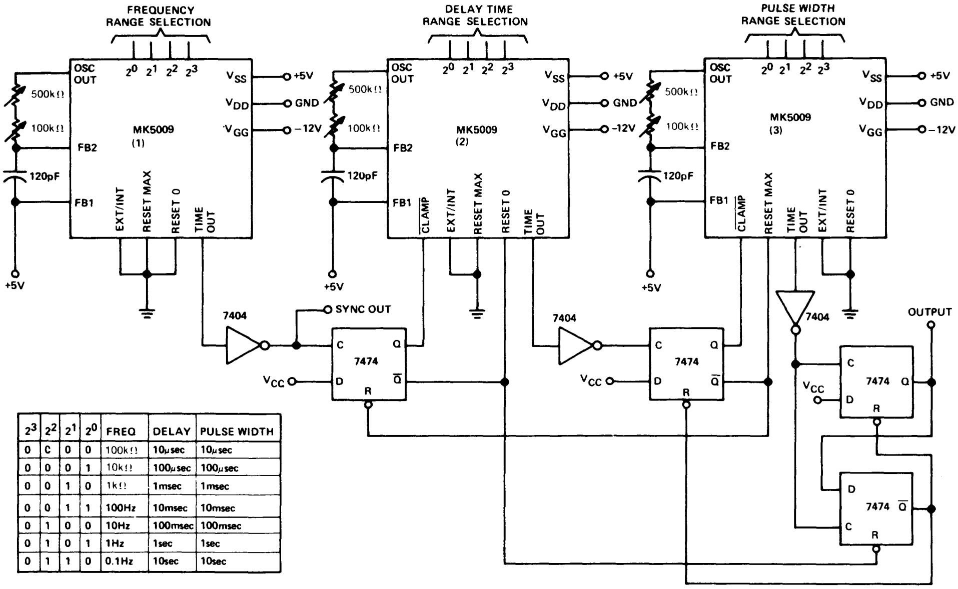


U1 – MK5009P
U2 – MK5002P/MK5005P
U3 – SCL4011

U4 – SCL4001
U5 – SCL4009
U6 – SCL4013

MISC. – 1.00MHz CRYSTAL,
LED DISPLAY
COMMON-CATHODE

PULSE GENERATOR



2^3	2^2	2^1	2^0	FREQ	DELAY	PULSE WIDTH
0	0	0	0	100kΩ	10μsec	10μsec
0	0	0	1	10kΩ	100μsec	100μsec
0	0	1	0	1kΩ	1msec	1msec
0	0	1	1	100Hz	10msec	10msec
0	1	0	0	10Hz	100msec	100msec
0	1	0	1	1Hz	1sec	1sec
0	1	1	0	0.1Hz	10sec	10sec

PULSE GENERATOR

An extremely versatile pulse generator requiring few components is easily built using the MK 5009. Three MK 5009 circuits are used, as shown in Figure 2, to provide the three essential pulse generator elements: (1) a frequency source to determine pulse repetition rate; (2) a variable time delay; and (3) a pulse width generator.

This circuit provides repetition rates from 0.1 Hz to 100 kHz with delay times and pulse widths from 10μ to 10 seconds. Range selection is obtained by selecting the appropriate dividers, so that only three RC circuits are required. This eliminates the requirement for a different RC combination for each decade, commonly found in commercial instruments. Decade selection is accomplished by a binary code at the inputs to each MK 5009, which could be provided by a coded rotary or thumbwheel switch. The vernier control is a 500k potentiometer. A 100k potentiometer is used as a trimmer for initial calibration. External TTL control logic is used to capture the accurately-controlled negative edges as they emerge from each MK 5009. The Reset and Clamp Inputs allow synchronization and first-cycle accuracy from the time-base circuits.

Other features can be added to the basic circuitry shown in Figure 2. For example, the output amplitude can be made adjustable by using high-voltage, open-collector TTL circuitry with potentiometer control for amplitude. An extra position can be used on the frequency selection switch for an external trigger source. This trigger source should be connected to the first control D-type latch in lieu of the output from the 5009 (1). The frequency range may even be extended to 1.0 MHz with time delays reduced to 1μs, although some loss in RC stability would occur since the recommended data sheet frequency has been exceeded.

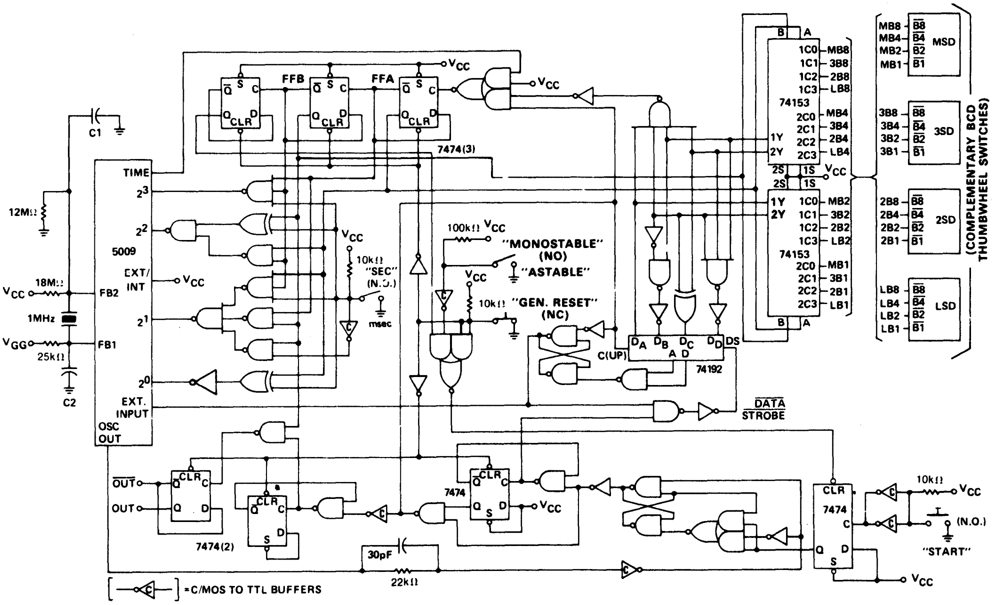
DIGITALLY-PROGRAMMABLE ONE-SHOT

Using the MK 5009 in the circuit shown in Figure 3 results in a very accurate one-shot which is digitally programmable. Four decades of thumbwheel switches allow pulse-width selection from 0.1 to 999.9 seconds, or 0.1 to 999.9 milliseconds, depending on the range selected. To indicate how the circuit functions, a general description of a typical one-shot application is used.

The user determines the required one-shot pulse width, for example 800.7 seconds. He must also determine desired output pulse polarity, i.e., (OUT or $\overline{\text{OUT}}$). The time is entered in the thumbwheel switch, the range switch is put in "Seconds", the mode select switch is put at "Monostable" and "Reset/Halt" is depressed momentarily.

To start the cycle, the "Start" button is depressed. This gates in the 1MHz clock from the MK 5009 through the C/MOS-to-TTL buffer. The first clock pulse is used to strobe the MSD into the variable-modulo counter (74192). (Actually the nine's complement is supplied to the counter through the BCD switch multiplex circuitry.) The ÷ N counter divides

DIGITALLY-PROGRAMMABLE ONE-SHOT



the 1 MHz clock by the integer value of the MSD. The states of flip-flops FFA and FFB determine which digit (or decade range) is being processed.

When the Time Out output from the MK 5009 completes its time cycle, it advances the state counter, selects the next digit to be processed, and then changes the variable modulo counter to correspond to this new digit. If the next digit happens to be a zero, the flip-flops (FFA and FFB) are toggled at the 1 MHz rate until a non-zero digit is found. In the example given (800.7 seconds) after timing of the 800 seconds is complete, the flip-flops would toggle through the second and third digits to ".7", the first non-zero digit, and count the remaining 7/10 second.

However, the one-shot may also be operated in an "astable" mode which results in a square-wave output with a period equal to twice the dial setting. Once the circuitry is started it will free-run until either the mode is changed or the Reset button is depressed.

Because of the synchronous nature of the MK 5009 counters, there should be no timing errors associated with the decade selection switching. The synchronous nature of the MK 5009 counters and processing the digits from MSD to LSD enables the circuit to operate without being reset and therefore does not introduce an additional time delay.

Further, the potential problem of timing errors at the beginning of a cycle is eliminated, since there is ample time (500 ns) to load a new digit integer code before the load command is taken away. This is true for either timing range, seconds or milliseconds.

FURTHER DESIGN APPLICATIONS

This basic design can be extended to accomplish a programmable sequence timer. Any kind of ROM (programmable, fixed mask, or diode matrix) can be used to contain all the times (BCD) codes for the required steps. A state counter of sufficient capacity can be used to control the addressing of the ROM.

Numerous applications for systems of this kind exist wherever a timed sequence of events is required, such as a photographic processing, process control, test sequences, and innumerable industrial applications.

USE WITH 2.0 MHz CRYSTAL

In some applications a different crystal frequency (such as 2.0 MHz) may be more readily available, although the actual requirements on the output might be decade divisions of 1.0 MHz. Figure 4 shows one way to accomplish this.

A 2.0 MHz crystal is used in the recommended circuit and the frequency at the Oscillator Output pin is divided by 2 by the flip-flop. The 1.0 MHz is then fed back into the chip at the External Input pin. The interface is constructed with C/MOS circuitry since it presents a very high input impedance which does not load down the oscillator output.

Use of C/MOS-to-TTL type inverters allows direct drive of the External input on the 5009 with its internal pull-up resistor.

This circuitry also provides a buffered 1.0 MHz (or 2.0 MHz) signal which can be used as a self-check input for a frequency meter without excessively loading the Oscillator Output.

USE WITH 2.0 MHz CRYSTAL

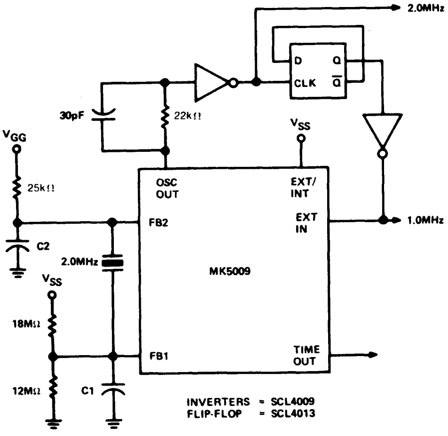


Figure 4

INTERNAL CONFIGURATION OF THE MK 5009 OSCILLATOR CIRCUIT

As can be seen in Figure 5 (a), the basic oscillator section of the MK 5009 is fairly simple. It consists of two parts: an active device, Q1, for gain in the crystal mode of operation; and a Schmitt trigger and inverting buffer for wave-shaping the waveform at Feedback 2.

In the RC oscillator mode, Figure 5 (b), Feedback 1 is tied to V_{SS}. This keeps Q1 off and effectively removes it from the circuit. One end of the timing capacitor and one end of the timing resistor are tied to Feedback 2. Osc. Out is connected to the other end of the resistor. The input at Feedback 2 is "squared-up", inverted, and used to drive Osc. Out, which causes the RC voltage waveform to change polarity. The nominal upper and lower trip points for the Schmitt trigger are −1.5V and −7.0V respectively.

In the crystal oscillator mode, Figure 5 (c), Q1 is used as the active device. A resistor, nominally 25kΩ, is placed from Feedback 2 to V_{GG}, serving as the load element for Q1. In practice the resistor should not have a value lower than 15kΩ. The RC product of this load resistor and the crystal loading capacitance should be smaller than $1/f_{XTAL}$, or the RC combination will affect the oscillator frequency. An inductance, or other external load network, can also be substituted for the load resistor. The device, Q1, has a width/length ratio of about 20 and a nominal g_m of 60 μmhos.

INTERNAL CONFIGURATION OF THE MK 5009 OSCILLATOR CIRCUIT

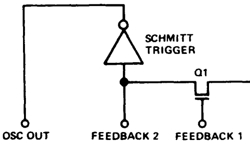


Figure 5 (a)

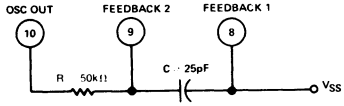


Figure 5 (b)

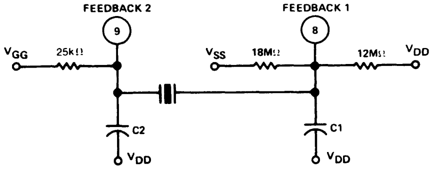


Figure 5 (c)

1980 INDUSTRIAL PRODUCTS DATA BOOK

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III Frequency Generator

IV Digital Alarm Clock

V Counter/Display Decoders

VI Counter/Time Base Circuit

VII A/D Converter/Analog Multiplexer

MOSTEK®

8-BIT A/D CONVERTER/8-CHANNEL ANALOG MULTIPLEXER

MK50808

FEATURES

- ☐ Single 5-Volt Supply (± 5%)
- ☐ Low Power Dissipation - 6.825mW(max) at 640kHz
- ☐ Total Unadjusted Error < ± ½ LSB
- ☐ Linearity Error < ± ½ LSB
- ☐ No Missing Codes
- ☐ Guaranteed Monotonicity
- ☐ No Zero Adjust Required
- ☐ No Full-Scale Adjust Required
- ☐ 108µs Conversion Time (Typically)
- ☐ Easy Microprocessor Interface
- ☐ Latched TTL-Compatible Three-State Output with True Bus-Driving Capability
- ☐ 8-channel Analog Multiplexer
- ☐ Latched Address Input
- ☐ Fixed Reference or Ratiometric Conversion
- ☐ Continuous or Controlled Conversion
- ☐ On-Chip Chopper-Stabilized Comparator
- ☐ Low Reference-Voltage Current Drain

DESCRIPTION

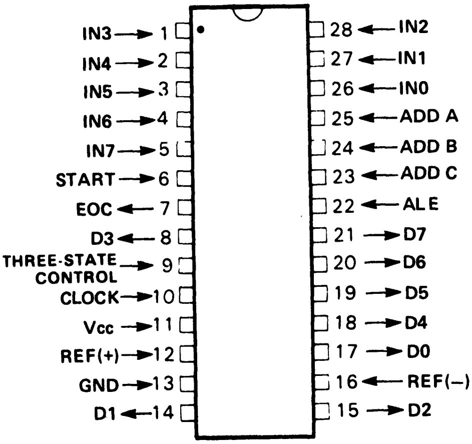
The MK50808 is a monolithic CMOS device with an 8-bit successive approximation A/D converter, an 8-channel analog multiplexer and microprocessor-compatible control logic. The 8-channel multiplexer can directly access any one of 8 single-ended analog channels. The 8-bit A/D converter consists of 256 series resistors with an analog switch array, a chopper-stabilized comparator and a successive approximation register. The series resistor approach guarantees monotonicity and no missing codes as well as allowing both ratiometric and fixed-reference measurements. The need for external zero and full-scale adjustments has been eliminated and an absolute accuracy of ⩽ 1 LSB, including quantizing error, is provided. A block diagram of the MK50808 is shown in Figure 2.

All digital outputs are TTL-compatible, all digital inputs are TTL-compatible with a pull-up resistor, and all digital inputs and outputs are CMOS-compatible; this makes it easy to interface with most microprocessors. The output latch is three-state and provides true bus-driving capability (300ns from Three-State Control to Q Logic State with 200pF load). A Start signal initiates the conversion process, and, upon completion, an End-Of-Conversion signal is generated. Continuous conversion is possible by tying the Start-Convert pin to the End-of-Conversion pin.

The pin configuration of the MK50808 is shown in Figure 1.

PIN CONNECTIONS

Figure 1

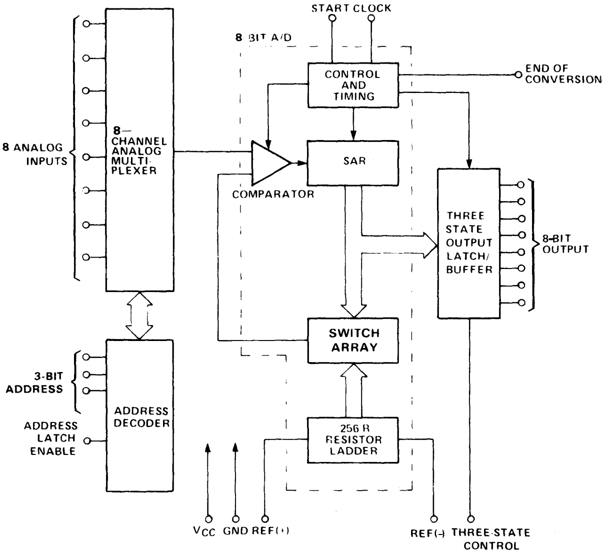


The MK50808 features low power, high accuracy, minimal temperature dependence, and excellent long-term accuracy and repeatability. These characteristics make this device ideally suited to machine and industrial controls.

A block diagram of a microprocessor control system using the MK50808 is shown in Figure 3.

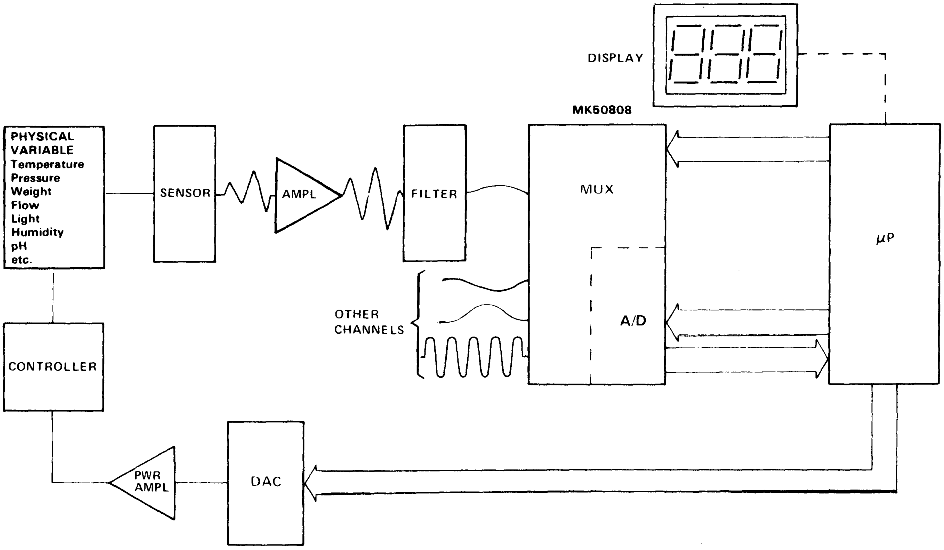
MK50808 BLOCK DIAGRAM

Figure 2



TYPICAL MICROPROCESSOR CONTROL SYSTEM

Figure 3



FUNCTIONAL DESCRIPTION (Refer To Figure 2 for a Block Diagram)

ADDRESS, Pins 23-25

The address decoder allows the 8-input analog multiplexer to select any one of 8 single-ended analog input channels. Table 1 shows the required address inputs to select any analog input channel.

ADDRESS LATCH ENABLE, Pin 22

A positive transition applied to the Address Latch Enable (ALE) input latches a 3-bit address into the address decoder. ALE can be tied to Start with parameter t_D being satisfied.

CLOCK INPUT, Pin 10

This Clock Input will accept an external clock input from 100kHz to 1.2MHz

POSITIVE AND NEGATIVE REFERENCE VOLTAGES [REF (+) and REF (-)], Pins 12 and 16

These inputs supply voltage references for the analog-to-digital converter. Internal voltage references are derived from REF (+) and REF (-) by a 256-R ladder network, Figure 4.

This approach was chosen because of its inherent monotonicity, which is extremely important in closed-loop feedback control systems. A non-monotonic transfer characteristic can cause catastrophic oscillations within a system.

The top and bottom resistors of the ladder network in Figure 4 are not the same value as the rest of the resistors in the ladder. They are chosen so that the output characteristic will be symmetrical about its full-scale and zero points. The first output transition occurs when the analog signal reaches +½ LSB and succeeding transitions occur every 1 LSB until the output reaches full scale.

ANALOG CHANNEL SELECTION

Table 1

SELECTED ANALOG CHANNEL	ADDRESS LINE			
		C	B	A
IN0		L	L	L
IN1		L	L	H
IN2		L	H	L
IN3		L	H	H
IN4		H	L	L
IN5		H	L	H
IN6		H	H	L
IN7		H	H	H

ANALOG INPUTS, Pins 1-5, 26-28

These inputs are multiplexing analog switches which accept analog inputs from 0V to V_{CC}.

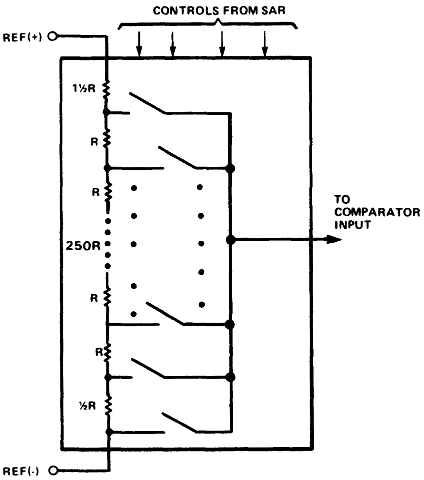
The comparator is the most important section of the A/D converter because this section determines the ultimate accuracy of the entire converter. It is the DC drift of the comparator which determines the repeatability of the device. A chopper-stabilized comparator was chosen because it best satisfies all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is amplified by a high-gain AC amplifier and the DC level is restored. This technique limits the drift component of the comparator because the drift is a DC component which is not passed by the AC amplifier.

Since drift is virtually eliminated, the entire A/D converter is extremely insensitive to temperature and exhibits very little long-term drift and input offset error.

RESISTOR LADDER AND SWITCH ARRAY

Figure 4



START, Pin 6

The A/D converter's successive approximation register (SAR) is reset by the positive edge of the Start pulse. Conversion begins on the falling edge of the Start pulse.

A conversion in progress will be interrupted if a new Start pulse is received and a new conversion will begin.

END OF CONVERSION, Pin 7

The End-Of-Conversion (EOC) output goes high when the conversion process has been completed. The positive edge of the EOC output indicates a valid digital output. Continuous conversion can be accomplished by tying the EOC output to the Start input. If the A/D converter is used in this mode, an external Start pulse should be applied after power up. End of Conversion will go low within 2 clock periods after the positive edge of Start.

8-BIT DIGITAL OUTPUT, Pins 8, 14, 15, 17-21

These pins supply the binary digital output code which corresponds to the analog input voltage. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). This output is stored in a TTL-compatible three-state output latch which can drive a 200pF bus from high impedance to either logic state in 300ns. Each pin can drive one standard TTL load.

THREE-STATE CONTROL, Pin 9

The Three-State Control allows the converter to be connected to an 8-bit data bus. A low level applied to this input causes the digital output to go to a high impedance state and a high level causes the output to go to a Q logic state.

ABSOLUTE MAXIMUM RATINGS* (Note 1)

Absolute Maximum V_{CC}	6.5V
Operating Temperature Range	MK50808 0°C to +70°C MK50808-1 -40° to +85°C
Storage Temperature Range	-65° to +150°C
Power Dissipation at 25°C	500mW
Voltage at any Pin except Digital Inputs	-0.3 to V_{CC} + 0.3V
Voltage at Digital Inputs	-0.3 to +15V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
MK50808, MK50808-1 (Note 1)

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	Measured at V_{CC} Pin	4.75	5.00	5.25	V	
V_{LADDER}	Voltage Across Ladder	From REF(+) to REF(-)	0.512	5.12	5.25	V	2
$V_{REF(+)}$	Voltage at Top of Ladder	Measured at REF(+)		V_{CC}	V_{CC}+0.1	V	
$\frac{\left(V_{REF(+)}+V_{REF(-)}\right)}{2}$	Voltage at Center of Ladder	Measured at $R_{LADDER}/2$	$\frac{V_{CC}}{2}$-0.1	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}$+0.1	V	
$V_{REF(-)}$	Voltage at Bottom of Ladder	Measured at REF(-)	-0.1	0		V	

DC CHARACTERISTICS

All parameters are 100% tested at 25°C. Device parameters are characterized at high and low temperature limits to assure conformance with the specification.

MK50808, MK50808-1

4.75 $\leq V_{CC} \leq$ 5.25V, -40 $\leq T_A \leq$ +85°C unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{INHIGH}	Logic Input High Voltage	V_{CC} = 5V	3.5			V	
V_{INLOW}	Logic Input Low Voltage	V_{CC} = 5V			1.5	V	
$V_{OUTHIGH}$	Logic Output High Voltage	I_{OUT} = -360μA	V_{CC} - 0.4			V	
V_{OUTLOW}	Logic Output Low Voltage	I_{OUT} = 1.6mA			0.4	V	
I_{INHIGH}	Logic Input High Current	V_{IN} = 15V			1.0	μA	
I_{INLOW}	Logic Input Low Current	V_{IN} = 0V	-1.0			μA	
I_{CC}	Supply Current	Clk. Freq=500kHz Clk. Freq=640kHz		300	1000 1300	μA μA	
I_{OUT}	Three-State Output Current	V_{OUT} = V_{CC} V_{OUT} = 0V	 -3		3 	μA μA	

DC CHARACTERISTICS

MK50808-1, -40 $\leq T_A \leq$ +85°C; MK50808, 0° $\leq T_A \leq$ +70°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
P_{SR}	Power Supply Rejection	4.75$\leq V_{CC} = V_{REF}(+)$ $\leq$5.25V;$V_{REF}(-)$=GND		0.05	0.15	%/V	10
R_{LADDER}	Ladder Resistance	From REF(+) to REF (-)	3.8	7		kΩ	

ANALOG MULTIPLEXER

MK50808, MK50808-1

-40° $\leq T_A \leq$ +85°C unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I_{ON}	On-Channel Input Current	f_C = 640kHz During Conversion	-2	± .05	+2	μA	11
$I_{OFF}(+)$	Off - Channel Leakage Current	V_{CC}=5V, V_{IN}=5V, T_A=25°C		10	200	nA	
$I_{OFF}(-)$	Off - Channel Leakage Current	V_{CC}=5V, V_{IN}=0V, T_A = 25°C	-200	-10		nA	

CONVERTER SECTION

$V_{CC} = V_{REF}(+) = 5V$, $V_{REF}(-) = GND$, $V_{IN} = V_{COMPARATOR\ IN}$, $f_C = 640kHz$
MK50808-1, $-40 \leq T_A \leq +85°C$ unless otherwise noted

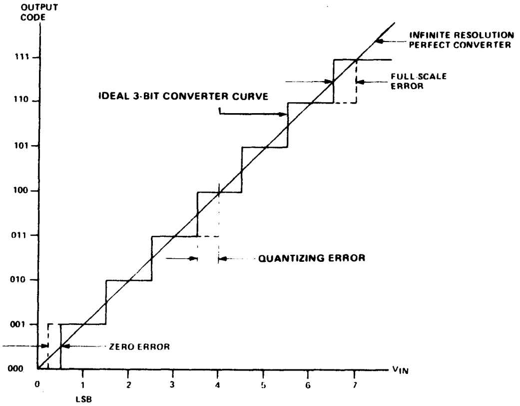
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Resolution				8	Bits	
Non-Linearity Error			± ¼	± ½	LSB	3
Zero Error			± ¼	± ½	LSB	5
Full-Scale Error			± ¼	± ½	LSB	6
Total Unadjusted Error	$T_A = 25°C$		± ¼ ± ¼	± ½ ± ¾	LSB LSB	7
Quantizing Error				±½	LSB	8
Absolute Accuracy	$T_A = 25°C$		± ¾ ± ¾	±1 ± 1¼	LSB LSB	9

MK50808, $0° \leq T_A \leq +70°C$

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Resolution			8	Bits	
Non-Linearity Error		± ½	± 1	LSB	3
Zero Error		± ¼	± ½	LSB	5
Full-Scale Error		± ¼	± ½	LSB	6
Total Unadjusted Error		± ½	± 1	LSB	7
Quantizing Error			± ½	LSB	8
Absolute Accuracy		± 1	± 1½	LSB	9

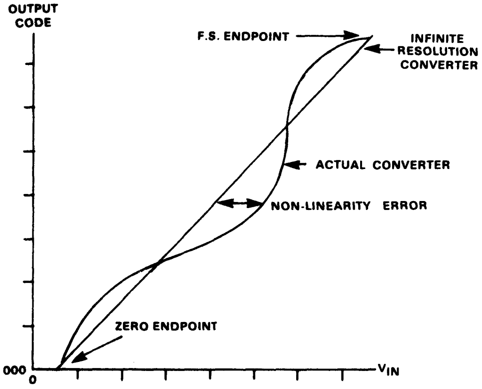
FULL-SCALE, QUANTIZING AND ZERO ERROR

Figure 5



NON-LINEARITY ERROR

Figure 6



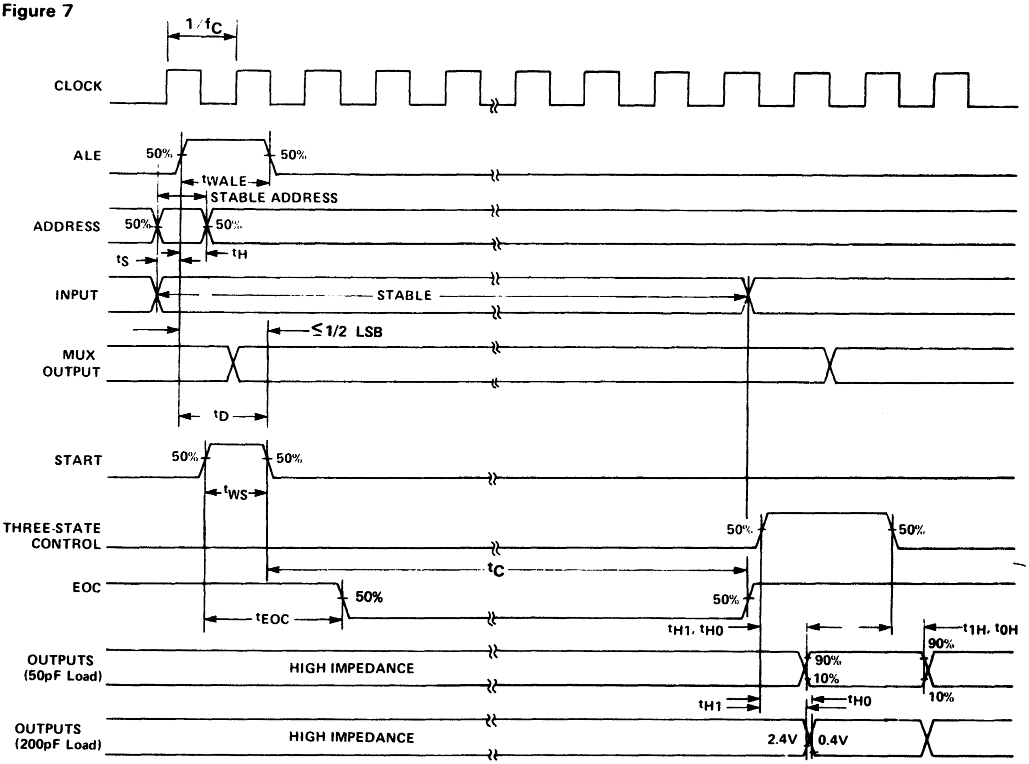
AC CHARACTERISTICS (Figure 7)

MK50808, MK50808-1, T_A = 25°C, $V_{CC} = V_{REF}(+)$ = 5V or 5.12V, $V_{REF}(-)$ = GND

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
t_{WS}	Start Pulse Width		200			ns	
t_{WALE}	Minimum ALE Pulse Width		200			ns	
t_S	Address Set-Up Time		50			ns	
t_H	Address Hold Time		50			ns	
t_D	Analog MUX Delay Time from ALE	$R_S + R_{ON} \leqslant 5k\Omega$		1	2.5	µs	12
t_{H1}, t_{H0}	Three-State Control to Q Logic State	C_L = 50pF C_L = 200pF		125	250 300	ns ns	
t_{1H}, t_{0H}	Three-State Control to Hi-Z	C_L = 10pF, R_L = 10kΩ		125	250	ns	
t_C	Conversion Time	f_C= 640kHz	106	108	110	µs	
f_C	External Clock Freq.		100	640	1200	kHz	
t_{EOC}	EOC Delay Time		0		2	Clock Periods	4
C_{IN}	Input Capacitance	At Logic Inputs At MUX Inputs		10 5	15 7.5	pF pF	
C_{OUT}	Three-State Output Capacitance	At Three-State Outputs		5	7.5	pF	

TIMING DIAGRAM

Figure 7



NOTES:

1. All voltages are measured with respect to GND.
2. The minimum value for V_{LADDER} will give 2mV resolution. However, the guaranteed accuracy is only that which is specified under "DC Characteristics"
3. Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer charecteristics, Figure 6.
4. When EOC is tied to START, EOC delay is 1 clock period.
5. Zero Error is the difference between the actual input voltage and the design input voltage which produces a zero output code, Figure 5.
6. Full-Scale Error is the difference between the actual input voltage and the design input voltage which produces a full-scale output code, Figure 5.
7. Total Unadjusted Error is the true measure of accuracy the converter can provide less any quantizing effects.
8. Quantizing Error is the ±½ LSB uncertainty caused by the converter's finite resolution, Figure 5.
9. Absolute Accuracy is the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code. This includes quantizing and all other errors.
10. Power Supply Rejection is the ability of an ADC to maintain accuracy as the power supply voltage varies. The power supply and $V_{REF}(+)$ are varied together and the change in accuracy is measured with respect to full-scale.
11. Input Current is the time average current into or out of the chopper-stabilized comparator. This current varies directly with clock frequency and has little temperature dependence.
12. This is the time required for the output of the analog multiplexer to settle within ±½ LSB of the selected analog input signal.

MOSTEK®

8-BIT A/D CONVERTER/16-CHANNEL ANALOG MULTIPLEXER

MK50816

FEATURES

- ☐ Single 5 Volt Supply (± 5%)
- ☐ Low Power Dissipation - 6.825mW(max) at 640kHz
- ☐ Total Unadjusted Error < ± ½ LSB
- ☐ Linearity Error < ± ½ LSB
- ☐ No Missing Codes
- ☐ Guaranteed Monotonicity
- ☐ No Zero Adjust Required
- ☐ No Full-Scale Adjust Required
- ☐ 108μs Conversion Time (Typically)
- ☐ Easy Microprocessor Interface
- ☐ Latched TTL Compatible Three-State Output with True Bus-Driving Capability
- ☐ Expandable 16-channel Analog Multiplexer
- ☐ Latched Address Input
- ☐ Fixed Reference or Ratiometric Conversion
- ☐ Continuous or Controlled Conversion
- ☐ On-Chip or External Clock
- ☐ On-Chip Chopper-Stabilized Comparator
- ☐ Low Reference-Voltage Current Drain

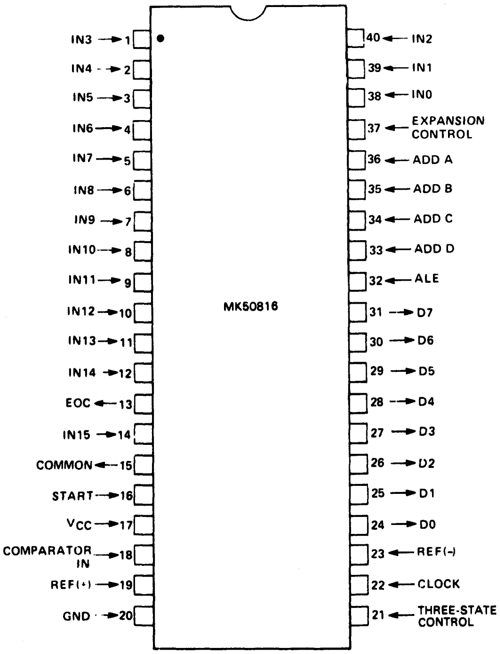
DESCRIPTION

The MK50816 is a monolithic CMOS device with an 8-bit successive approximation A/D converter, a 16-channel analog multiplexer and microprocessor-compatible control logic. The 16-channel multiplexer can directly access any one of 16 single-ended analog channels and provides logic for additional channel expansion. The 8-bit A/D converter consists of 256 series resistors with an analog switch array, a chopper-stabilized comparator and a successive approximation register. The series resistor approach guarantees monotonicity and no missing codes as well as allowing both ratiometric and fixed-reference measurements. The need for zero and full-scale adjustments has been eliminated and an absolute accuracy of ≤ 1 LSB, including quantizing error, is provided.

The pin configuration of the MK50816 is shown in Figure 1 below:

PIN CONNECTIONS

Figure 1



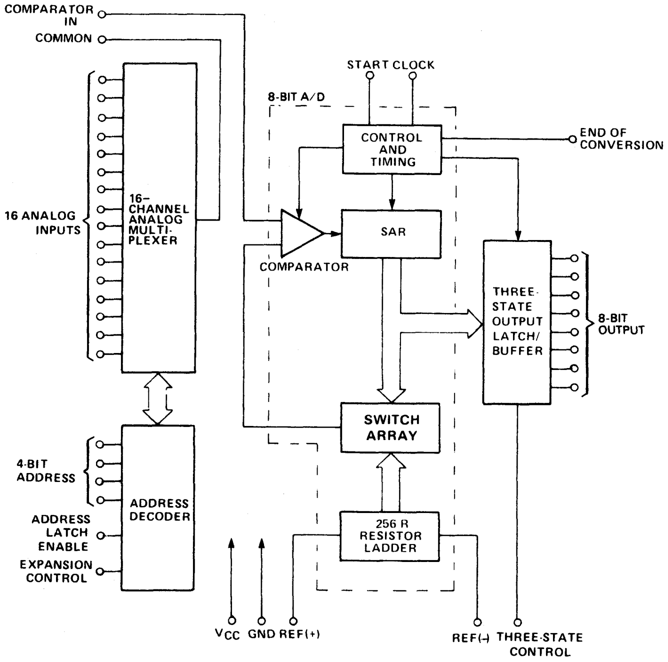
All digital outputs are TTL-compatible, all digital inputs are TTL-compatible with a pull-up resistor, and all digital inputs and outputs are CMOS-compatible; this makes it easy to interface with most microprocessors. The output latch is three-state and provides true bus-driving capability (300ns from Three-State Control to Q Logic State with 200pF load). A Start Convert signal initiates the conversion process, and, upon completion, an End Of Conversion signal is generated. Continuous conversion is possible by tying the Start-Convert pin to the End-of-Conversion pin. The clock pin may be connected to an external oscillator or tied to ground to enable an on-chip oscillator.

The MK50816 features low power, high accuracy, minimal temperature dependence, and excellent long-term accuracy and repeatability. These characteristics make this device ideally suited to machine and industrial controls.

A block diagram of a microprocessor control system using the MK50816 is shown in Figure 3.

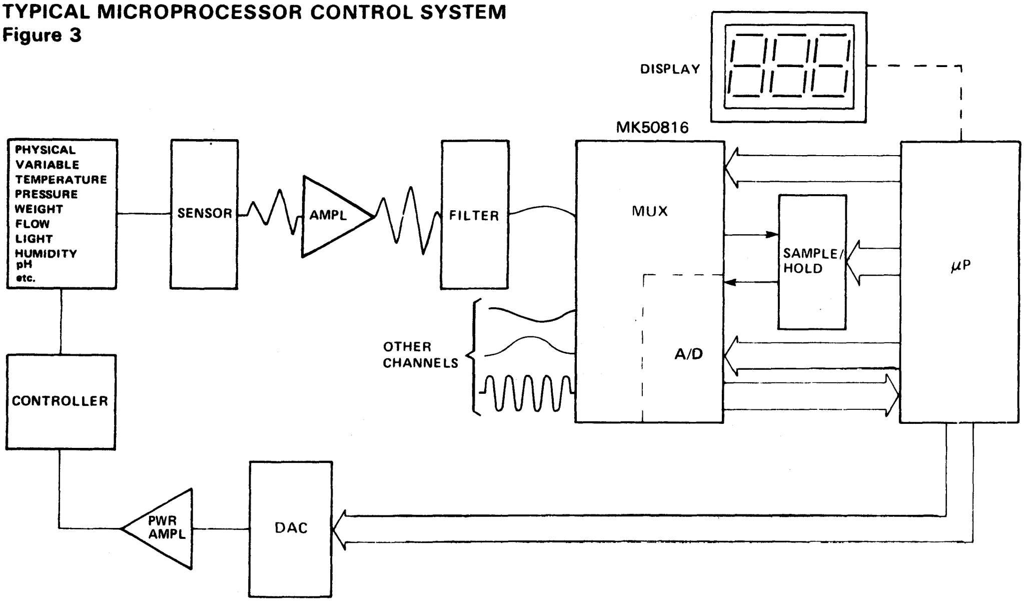
MK50816 BLOCK DIAGRAM

Figure 2



TYPICAL MICROPROCESSOR CONTROL SYSTEM

Figure 3



FUNCTIONAL DESCRIPTION (Refer To Figure 2 for a Block Diagram)

ADDRESS, Pins 33-36

The address decoder allows the 16-input analog multiplexer to select any one of 16 single-ended analog input channels. Table 1 shows the required address and expansion control inputs to select any analog input channel.

ADDRESS LATCH ENABLE, Pin 32

A positive transition applied to the Address Latch Enable (ALE) input latches a 4-bit address into the address decoder. ALE can be tied to Start with parameter t_D being satisfied.

COMMON OUTPUT, Pin 15

This is the output of the 16-channel analog multiplexer. The maximum ON resistance is 3kΩ.

EXPANSION CONTROL, Pin 37

Additional single-ended analog signals can be multiplexed to the A/D converter by holding the Expansion Control low, disabling the multiplexer. These additional externally-multiplexed signals are to be connected to the Comparator Input and the device ground. Additional signal conditioning such as sample-and-hold or instrumentation amplification can be added between the analog signal and the Comparator Input.

ANALOG CHANNEL SELECTION
Table 1

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

CLOCK INPUT, Pin 22

The Clock Input will accept an external clock input from 100kHz to 1.2MHz. A minimum duty cycle of 20% is required for the Clock Input to detect the presence of an external clock signal.

If the Clock pin is grounded, the conversion process will be controlled by an on-chip oscillator.

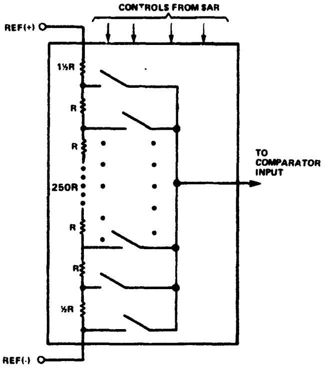
POSITIVE AND NEGATIVE REFERENCE VOLTAGES [REF (+) and REF (-)], Pins 19 and 23

These inputs supply voltage references for the analog-to-digital converter. Internal voltage references are derived from REF (+) and REF (-) by a 256-R ladder network, Figure 4.

This approach was chosen because of its inherent monotonicity, which is extremely important in closed-loop feedback control systems. A non-monotonic transfer characteristic can cause catastrophic oscillations within a system.

The top and bottom resistors of the ladder network in Figure 4 are not the same value as the rest of the resistors in the ladder. They are chosen so that the output characteristic will be symmetrical about its full-scale and zero points. The first output transition occurs when the analog signal reaches +½ LSB and succeeding transitions occur every 1 LSB until the output reaches full scale.

RESISTOR LADDER AND SWITCH ARRAY
Figure 4



ANALOG INPUTS, PINS 1-12, 14, 38-40

These inputs are multiplexing analog switches which accept analog inputs from 0V to V_{CC}.

COMPARATOR INPUT, Pin 18

The comparator is the most important section of the A/D converter because this section determines the ultimate accuracy of the entire converter. It is the DC drift of the comparator which determines the repeatability of the device. A chopper-stabilized comparator was chosen because it best satisfies all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is amplified by a high-gain AC amplifier and the DC level is restored. This technique limits the drift component of the comparator because the drift is a DC component which is not passed by the AC amplifier.

Since drift is virtually eliminated, the entire A/D converter is extremely insensitive to temperature and exhibits very little long-term drift and input offset error.

START, Pin 16

The A/D converter's successive approximation register (SAR) is reset by the positive edge of the Start pulse. Conversion begins on the falling edge of the Start pulse. A conversion in progress will be interrupted if a new start conversion pulse is received and a new conversion will begin.

END OF CONVERSION, Pin 13

The End Of Conversion (EOC) output goes high when the conversion process has been completed. The positive edge of the EOC output indicates a valid digital output. Continuous conversion can be accomplished by tying the EOC output to the Start input. If the A/D converter is used in this mode, an external start conversion pulse should be applied after power up. End of Conversion will go low within 2 clock periods after the positive edge of Start.

8-BIT DIGITAL OUTPUT, Pins 24-31

These pins supply the digital output code which corresponds to the analog input voltage. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). This output is stored in a TTL-compatible three-state output latch which can drive a 200pF bus from high impedance to either logic state in 300ns. Each pin can drive one standard TTL load.

THREE-STATE CONTROL, Pin 21

The Three-State Control allows the converter to be connected to an 8-bit data bus. A low level applied to this input causes the digital output to go to a high impedance state and a high level causes the output to go to a Q logic state.

ABSOLUTE MAXIMUM RATINGS* (Note 1)

Absolute Maximum V_{CC}	6.5V
Operating Temperature Range	MK50816 0° to +70°C MK50816-1 -40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation at 25°C	500mW
Voltage at any Pin except Digital Inputs	-0.3 to V_{CC} + 0.3V
Voltage at Digital Inputs	-0.3 to +15V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
MK50816, MK50816-1 (Note 1)

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	Measured at V_{CC} Pin	4.75	5.00	5.25	V	
V_{LADDER}	Voltage Across Ladder	From REF(+) to REF (-)	0.512	5.12	5.25	V	2
$V_{REF}(+)$	Voltage at Top of Ladder	Measured at REF (+)		V_{CC}	$V_{CC}+0.1$	V	
$\frac{\left(V_{REF}(+) + V_{REF}(-)\right)}{2}$	Voltage at Center of Ladder	Measured at $R_{LADDER}/2$	$\frac{V_{CC}}{2} - 0.1$	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2} + 0.1$	V	
$V_{REF}(-)$	Voltage at Bottom of Ladder	Measured at REF(-)	-0.1	0		V	

DC CHARACTERISTICS

All parameters are 100% tested at 25°C. Device parameters are characterized at low and high temperature limits to assure conformance with the specification.

MK50816, MK50816-1

$4.75 \leq V_{CC} \leq 5.25V$, $-40 \leq T_A \leq +85°C$ unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{INHIGH}	Logic Input High Voltage	$V_{CC} = 5V$	3.5			V	
V_{INLOW}	Logic Input Low Voltage	$V_{CC} = 5V$			1.5	V	
$V_{OUTHIGH}$	Logic Output High Voltage	$I_{OUT} = -360\mu A$	$V_{CC} - 0.4$			V	
V_{OUTLOW}	Logic Output Low Voltage	$I_{OUT} = 1.6mA$			0.4	V	
I_{INHIGH}	Logic Input High Current	$V_{IN} = 15V$			1.0	μA	
I_{INLOW}	Logic Input Low Current	$V_{IN} = 0V$	-1.0			μA	
I_{CC}	Supply Current	Clk Freq=500kHz Clk Freq=640kHz		300	1000 1300	μA μA	
I_{OUT}	Three-State Output Current	$V_{OUT}=V_{CC}$ $V_{OUT}=0V$	 -3		3 	μA μA	

DC CHARACTERISTICS

MK50816-1 $-40 \leq T_A \leq +85°C$, MK50816 $0° \leq T_A \leq +70°C$

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
R_{PS}	Power Supply Rejection	$4.75 \leq V_{CC} \leq 5.25$ $V_{REF}(+) = V_{CC}$ $V_{REF}(-) = GND$		0.05	0.15	%/V	10
$I_{COMP\ IN}$	Comparator Input Current	$f_C = 640kHz$ During Convs.	-2	±0.5	2	μA	11
R_{LADDER}	Ladder Resistance	From REF(+) to REF (-)	3.8	7		kΩ	

ANALOG MULTIPLEXER
MK50816, MK50816-1
$-40° \leq T_A \leq +85°C$ unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) $T_A = 25°C$, $R_L = 10k$		1.5	3	kΩ	
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10k$		75		Ω	
$I_{OFF}(+)$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=5V$, $T_A=25°C$		10	200	nA	
$I_{OFF}(-)$	OFF Channel Leakage Current	$V_{CC}=5V$, $V_{IN}=0V$, $T_A=25°C$	-200	-10		nA	

CONVERTER SECTION
$V_{CC} = V_{REF}(+) = 5V$, $V_{REF}(-) = GND$, $V_{IN} = V_{COMPARATOR\ IN}$,
$f_C = 640kHz$
MK50816-1 $-40 \leq T_A \leq +85°C$ unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Resolution				8	Bits	
Non-Linearity Error			± ¼	± ½	LSB	3
Zero Error			± ¼	± ½	LSB	5
Full-Scale Error			± ¼	± ½	LSB	6
Total Unadjusted Error	$T_A = 25°C$		± ¼ ± ¼	± ½ ± ¾	LSB LSB	7
Quantizing Error				± ½	LSB	8
Absolute Accuracy	$T_A = 25°C$		± ¾ ± ¾	± 1 ± 1¼	LSB LSB	9

MK50816 $0° \leq T_A \leq +70°C$

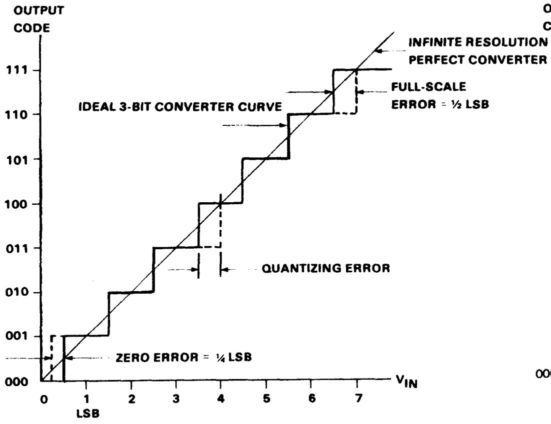
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Resolution				8	Bits	
Non-Linearity Error			± ½	± 1	LSB	3
Zero Error			± ¼	± ½	LSB	5
Full-Scale Error			± ¼	± ½	LSB	6
Total Unadjusted Error			± ½	± 1	LSB	7
Quantizing Error				± ½	LSB	8
Absolute Accuracy			± 1	± 1½	LSB	9

AC CHARACTERISTICS (Figure 7)

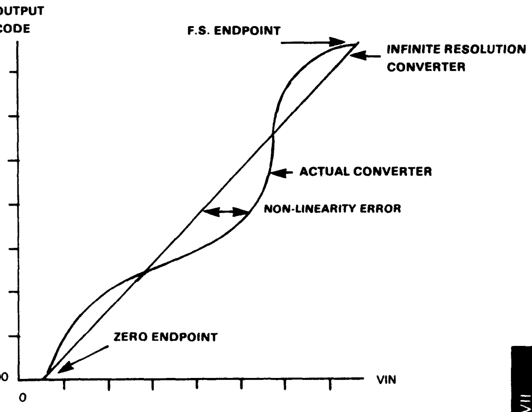
MK50816, MK50816-1 $T_A = 25°C$, $V_{CC} = V_{REF}(+) = 5V$ or 5.12V, $V_{REF}(-) = GND$

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
t_{WS}	Start Pulse Width		200			ns	
t_{WALE}	Minimum ALE Pulse Width		200			ns	
t_S	Address Set-Up Time		50			ns	
t_H	Address Hold Time		50			ns	
t_D	Analog MUX Delay Time from ALE	Common Tied to Comparator In, $R_S + R_{ON} \leq 5k\Omega$, $C_L = 10pF$		1	2.5	µs	12
t_{H1}, t_{H0}	Three-State Control to Q Logic State	$C_L = 50pF$ $C_L = 200pF$		125 300	250	ns ns	
t_{1H}, t_{0H}	Three-State Control to Hi-Z	$C_L = 10pF$, $R_L = 10k\Omega$		125	250	ns	
t_C	Conversion Time	$f_C = 640kHz$ $f_C = f_{INTERNAL\ CLOCK}$	106	108 150	110	µs µs	
f_C	External Clock Freq		100	640	1200	kHz	13
t_{EOC}	EOC Delay Time		0		2	Clock Periods	4
C_{IN}	Input Capacitance	At Logic Inputs At MUX Inputs		10 5	15 7.5	pF pF	
C_{OUT}	Three-State Output Capacitance	At Three-State Outputs		5	7.5	pF	

FULL SCALE, QUANTIZING AND ZERO ERROR
Figure 5

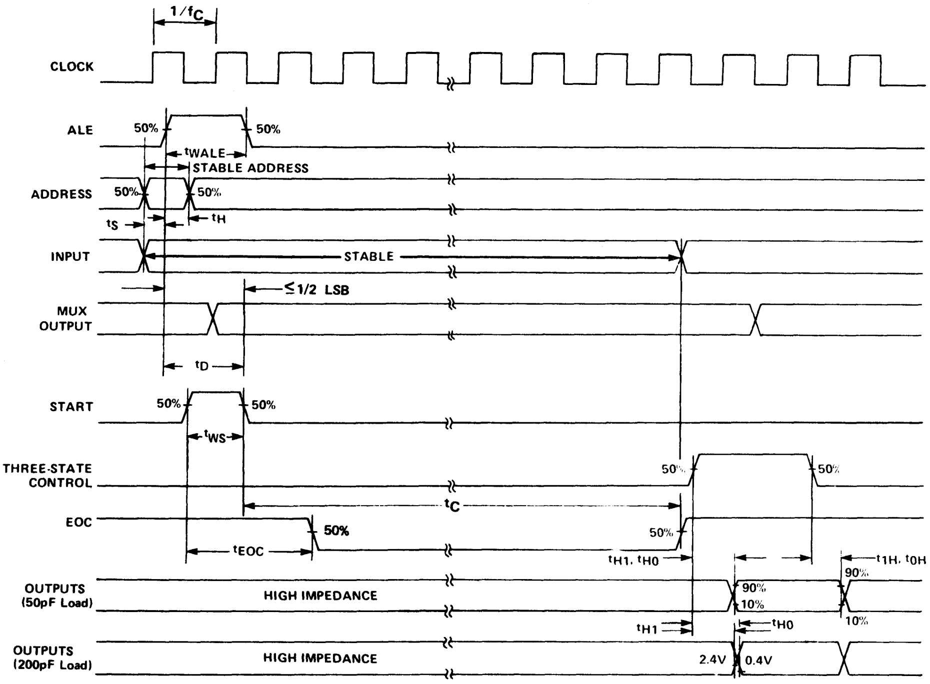


NON-LINEARITY ERROR
Figure 6



TIMING DIAGRAM

Figure 7



NOTES:

1. All voltages are measured with respect to GND.
2. The minimum value for V_{LADDER} will give 2mV resolution. However, the guaranteed accuracy is only that which is specified under "DC Characteristics".
3. Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic, Figure 6.
4. When EOC is tied to START, EOC delay is 1 clock period.
5. Zero Error is the difference between the actual input voltage and the design input voltage which produces a zero output code, Figure 5.
6. Full-Scale Error is the difference between the actual input voltage and the design input voltage which produces a full-scale output code, Figure 5.
7. Total Unadjusted Error is the true measure of accuracy the converter can provide less any quantizing effects.
8. Quantizing Error is the ± ½ LSB uncertainty caused by the converter's finite resolution, Figure 5.
9. Absolute Accuracy is the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code. This includes quantizing and all other errors.
10. Power Supply Rejection is the ability of an ADC to maintain accuracy as the power supply voltage varies. The power supply and $V_{REF}(+)$ are varied together and the change in accuracy is measured with respect to full-scale.
11. Comparator Input Current is the time average current into or out of the chopper-stabilized comparator. This current varies directly with clock frequency and has little temperature dependence.
12. This is the time required for the output of the analog multiplexer to settle within ± ½ LSB of the selected analog input signal.
13. A minimum duty cycle of 20% is required at the clock input.

NOTES

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